onsemi M 1 1200 V SiC MOSFETs & Modules: Characteristics and Driving Recommendations

AND90103/D

ABSTRACT

SiC MOSFETs are quickly proliferating in the power semiconductor market as some of the initial reliability concerns have been resolved and the price level has reached a very attractive point. As more devices become available in the market, it is important to understand both the commonalities and the differences with IGBTs so that the user can get the most out of each device. This paper provides an overview on the key characteristics of **onsemi** M 1 1200 V SiC MOSFETs and how they can be influenced by the driving conditions. As part of the full wide bandgap ecosystem that **onsemi** offers, this article also provides a guideline on the usage of the NCP51705 an isolated gate driver for SiC MOSFETs.

INTRODUCTION

Silicon carbide (SiC) is part of the wide bandgap (WBG) family of semiconductor materials used to fabricate discrete power semiconductors. As shown in Table 1, conventional silicon (Si) MOSFETs have a bandgap energy of 1.12 eV compared to SiC MOSFETs possessing 3.26 eV.

The wider bandgap energy associated with SiC and (GaN) Gallium Nitride means that it takes approximately 3 times the energy to move electrons from their valence band to the conduction band, resulting in a material that behaves more like an insulator and less like a conductor. This allows WBG semiconductors to withstand much higher breakdown voltages, highlighted by their breakdown field robustness being 10 times that of silicon. A higher breakdown field enables a reduction in device thickness for a given voltage rating which translates to lower on−resistance and higher current capability. SiC and GaN each have mobility parameters on the same order of magnitude as silicon, making both materials well suited for high−frequency switching applications. The thermal conductivity of SiC is three times greater than that of silicon and GaN. Higher thermal conductivity translates to lower temperature rise for a given power dissipation.

The $R_{DS(ON)}$ for a specific required breakdown voltage considering one part of a MOSFET [1] is inversely proportional to the product of the mobility times the cube of the critical breakdown field. Even if SiC has a lower mobility than silicon, the critical breakdown field is ten times higher, resulting in a much lower $R_{DS(ON)}$ for a given breakdown voltage.

The guaranteed maximum operating temperature for commercially available SiC MOSFETs is $150°C < T_J < 200°C$. Comparatively, SiC junction temperatures as high as 600°C are attainable but mostly limited by bonding and packaging techniques. This makes SiC the superior WBG semiconductor material for high−voltage, high−speed, high−current, high−temperature, switching power applications.

Table 1. SEMICONDUCTOR MATERIAL PROPERTIES

Properties	Si	4H − SiC	GaN
Band Energy (eV)	1.12	3.26	3.50
Electron Mobility (cm^2/Vs)	1400	900	1250
Hole Mobility (cm^2/Vs)	600	100	200
Breakdown Filed (MV/cm)	0.3	3.0	3.0
Thermal Conductivity (W/cm °C)	1.5	4.9	1.3
Maximum Junction Temperature (°C)	150	600	400

SiC MOSFETs are commonly available in the range of 650 V < BVDSS < 1.7 kV. Although the dynamic switching behavior of SiC MOSFETs is quite similar to standard silicon MOSFETs, there are unique gate drive requirements dictated by their device characteristics that must be taken into consideration.

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STATIC CHARACTERISTICS

Blocking Voltage Capability

onsemi M 1 1200 V SiC MOSFETs are rated at 1200 V with a maximum Zero Gate Voltage Drain Current (I_{DSS}) that is specified in the datasheet of each specific device. However, the blocking voltage capability of a SiC MOSFET will reduce with temperature. Taking as an example a 1200 V 20 mΩ SiC MOSFET power module, the typical derating in the blocking voltage (V_{DS}) at −40°C is around 11% compared to the value at 25°C. Even if **onsemi** devices have typically some margin, the derating in the V_{DS} should be considered during the design, especially if the device will operate at extremely low temperatures. In Figure 1 the typical distribution of the breakdown voltages vs. temperature can be seen.

Important note: These are typical reference values and not guaranteed, please refer to datasheet values or contact your local technical support.

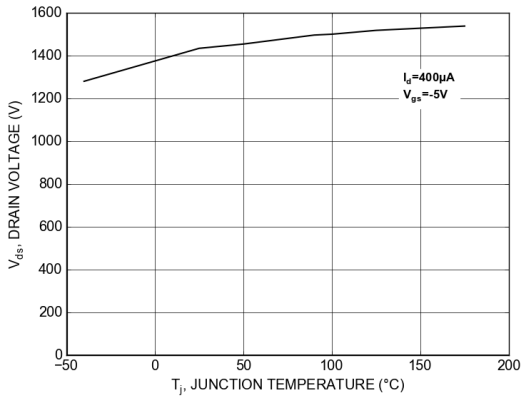

Figure 1. Typical Distribution of V_{DS} vs. Temperature

$R_{DS(ON)}$ Characteristics and Recommended V_{GS} to Drive onsemi M 1 1200 V SiC MOSFETs

One of the key differentiators of a SiC MOSFET compared to their Si relatives is the dependency of the Drain to Source Voltage (V_{DS}) vs. the Gate Source Voltage (V_{GS}) for a specific Drin Current (I_D) and in this **onsemi** 1200 V SiC MOSFETs are no exception. Figure 2 shows that traditional Si MOSFETs show a clear transition between the linear (ohmic) and the active region (saturation). On the other hand, looking at Figure 3, SiC MOSFETs do not show this behavior and in fact, there is no saturation region, which means that a SiC MOSFET behaves more like a variable resistance rather than a non−ideal current source.

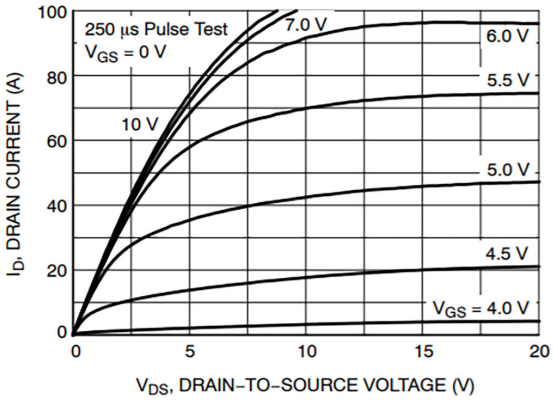

Figure 2. Typical Static Characteristics of a SJ MOSFET

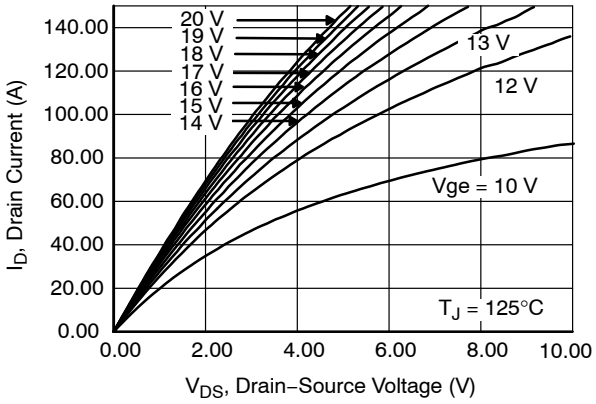

Figure 3. Typical Static Characteristics of onsemi 1200 V SiC MOSFET M 1

One important aspect to consider when selecting the appropriate V_{GS} is that unlike their Si counterpart, SiC MOSFETs will continue to show a significant improvement in the $R_{DS(ON)}$ when the V_{GS} is increased even at relatively high voltages. This can be observed in Figure 3: the curve moves to the left as V_{GS} is increased. If we take look at Figure 2, the $R_{DS(ON)}$ of the Si MOSFET does not show a significant improvement when $V_{GS} >> V_{Th}$, for this reason

most Si MOSFET are typically driven with a $V_{GS} \leq 10$ V. For this reason, if were to replace a Si MOSFET by a SiC one, a modification of the driving voltage is recommended. Although 10 V is above the typical threshold voltage of a SiC MOSFET, the conduction losses at such a low V_{GS} would most likely lead to a thermal runaway of the device. This is one of the reasons why a $V_{GS} \geq 18$ V is recommended to drive **onsemi** 1200 V M 1 SiC MOSFETs.

If the voltage selected is too high, that would introduce a higher stress in the gate oxide that might lead to long−term reliability issues or the change in critical characteristics such as a drift in the V_{TH}. During the qualification phase, **onsemi** M 1 1200 V SiC MOSFETs have gone through an extensive set of tests in order to specify a maximum gate voltage of + 25 V. As an example, in Figure 4 the results of the positive gate bias stress test can be observed in green. Compared to other vendors, **onsemi** M 1 1200 V SiC MOSFETs show a good stability when + 25 V is constantly applied.

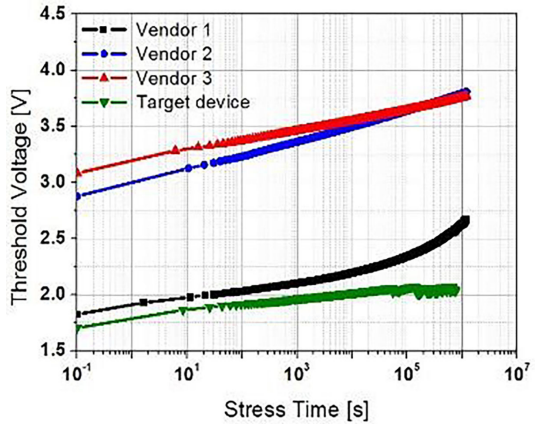

Figure 4. Positive Gate Bias Stress Test. Test Conditions: V_{GS} = 25 V, T = 175°C

Even in the best layouts and the least inductive packages, transient voltage spikes at the gate of the die cannot be avoided. In order to not surpass the barrier of + 25 V, it is recommended that a maximum constant voltage of $V_{GS} \leq 20$ V is applied to the MOSFET.

$R_{DS(ON)}$, Temperature Dependency

Another factor to consider is the temperature coefficient of SiC MOSFETs. At low temperatures, a SiC MOSFET typically presents a negative temperature coefficient (NTC) until it reaches a certain temperature in which it starts having a positive temperature coefficient (PTC). This turning point is influenced by the $V_{GS,}$ At lower V_{GS} the NTC is dominant up to higher temperatures, while if this voltage is increased, the turning point will happen at lower temperatures. In Figure 5 the typical dependency of the $R_{DS(ON)}$ vs. temperature at different V_{GS} of **onsemi** M 1 SiC MOSFETs can be observed. If we look at the curve at V_{GS} = 15 V, the NTC is very steep at negative temperatures and remains dominant up to 50°C approximately which leads to the fact that the $R_{DS(ON)}$ for high temperatures remains in all cases lower than the $R_{DS(ON)}$ at negative temperatures. If two components are switched in parallel, like it is the case of many of our power modules, one of the components could end up being overloaded, especially if the device starts at negative ambient temperatures, leading to a possible thermal runaway. This phenomenon is corrected if the V_{GS} is increased. At 18 V, the turning point of the temperature coefficient is at approximately 25°C and at 100°C the $R_{DS(ON)}$ value is already higher than at −40°C, what makes it a safe voltage to switch devices in parallel even if they are used in cold environments.

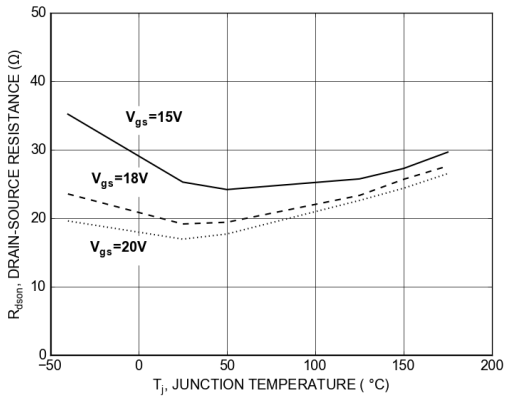

Figure 5. Temperature Dependency of $R_{DS(ON)}$ at Different V_{GS}

In order to calculate the static losses of a SiC MOSFET device or when different vendors are compared, it is important to look at the $R_{DS(ON)}$ of the device not only at 25°C, often used to define the devices for marketing purposes, but at the $R_{DS(ON)}$ at the target application temperature. As explained in the previous paragraph, after a certain turning point, SiC MOSFETs have a PTC. The benefits of this have been already explained, however, if the coefficient is very high, the difference between the $R_{DS(ON)}$ at 25°C and real temperature in the application can become critical, leading to significantly higher conduction losses at the target operating temperatures. This needs to be considered when selecting a SiC MOSFET.

onsemi M 1 1200 V SiC MOSFETs show a good stability in the $R_{DS(ON)}$ when the temperature is increased. Figure 6 shows the difference at 25°C and 150°C of a 20 mΩ device for different Drain currents (I_D). At I_D = 50 A, there is a 33% increase in the $R_{DS(ON)}$, which is enough to ensure good parallel operation without drastically increasing the static losses.

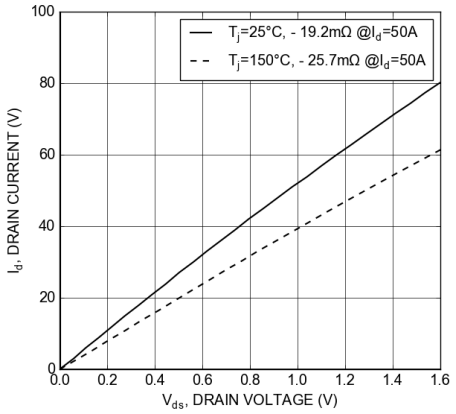

Figure 6. VDS vs. ID at Different Temperatures of a 1200 V, 20 mΩ SiC MOSFET Power Module

Selecting the Negative Gate Bias Voltage

So far, the different parameters to define the positive gate bias have been discussed. The conclusion is that the V_{GS} for **onsemi** M 1 1200 V SiC MOSFETs should be set to + 18 V ≤ V_{GS} ≤ 20 V during static operation and that it should not surpass + 25 V in the dynamic transients, but how to define the negative gate bias? Certainly, this value should be low enough to guarantee that the device switches off properly, but also to avoid a parasitic turn on in those topologies that are susceptible to shoot−through like a half−bridge.

Currently two types of SiC MOSFETs can be found in the market in terms of V_{TH}, high threshold voltage SiC MOSFETs with typical values above 3.5 V and lower threshold voltage SiC MOSFETs with typical values below 3 V to 3.5 V. **onsemi** M 1 1200 V SiC MOSFETs belong to the second group with a typical V_{TH} values in the range of 2.75 V (see datasheet for specific values of each device). This value varies with the temperature and could go as low as 1.8 V and as high as 4.3 V.

In those applications in which shoot−through could happen a negative gate bias of − 5 V is recommended to have enough safety margin to avoid parasitic turn on, especially at high switching frequencies. Setting the negative V_{TH} to − 5 V should also give enough margin to avoid transient gate voltages below the minimum limit which is set at −15 V.

In those cases in which the risk of shoot−through is non−existing, i.e. a booster topology, or has been reduced by one of the many existing techniques, i.e. decoupling the output of a half−bridge with a parasitic inductance, then the negative gate bias could be increased to any safe value going as high as 0 V. This has other effects on the performance of the device that will be discussed in the next chapter.

Just like with the positive gate bias, having a very low negative gate bias might trigger defects of the SiC crystal, leading to reliability issues or the modification of key parameters such as a drift in the V_{TH} or the $R_{DS(ON)}$, this is especially critical when talking about negative gate bias and the currently available SiC trench MOSFETs. In order to prevent these issues, **onsemi** has considered this in the design and has done extensive static and dynamic tests of the M 1 1200 V SiC MOSFETs to confirm there is no drift. Figure 7 shows as example the results of the static negative gate bias and its influence in the V_{TH}. On top of this, burn−in tests are conducted in our production line to limit premature failures.

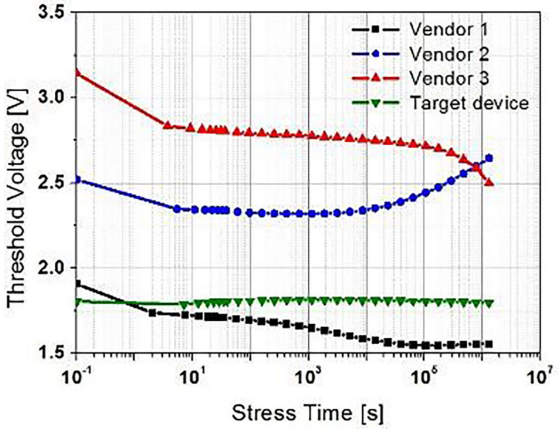

Figure 7. Negative Gate Bias Stress Test. Test Conditions: V_{GS} = −20 V, T = 175 °C

Body Diode Forward Voltage (V_f) vs. V_{GS}

The body diode of SiC MOSFETs is well−known for having a high forward voltage compared to other types of diodes. This characteristic should be considered when using a SiC MOSFET and in general, it is not recommended to use it outside the dead time in many topologies to avoid high losses. One effective way to reduce the usage of the body diode is to activate the channel of the MOSFET when reverse conduction is needed. By doing this the losses will be drastically reduced.

However, in those topologies in which a dead time is needed before activating the channel, i.e. a typical half−bridge in synchronous rectification, the de−activation of the body diode becomes ineffective as additional devices and/or modifications in the current path would be required. Moreover, even taking many precautions the utilization of the body diode during the dead time might not be fully avoided. In case of **onsemi** M 1 1200 V SiC MOSFETs, the body diode can be used without a penalty in reliability or a big drift in the main parameters of the MOSFET.

Having this in mind, it is important to know that the V_{GS} will have an influence in the static performance of the body diode. Figure 8 shows the V_f dependency of **onsemi** M 1 1200 V SiC MOSFET's body diode vs. the forward current (I_f), when a different V_{GS} is applied. As it can be observed, the V_f increases slightly when the negative gate bias is reduced. This graphic is a bit misleading as it could bring the user to the conclusion that setting a V_{GS} to 0 V is the best solution. However, the reason for this lower V_f is that the channel of the MOSFET turns slightly on, so what it looks externally like a lower V_f is actually the channel taking part of the current from the body diode. When the diode stops conducting, the channel will remain slightly on. Depending

on the switching topology, this could have a negative effect in the total losses with an increased leakage. On top of this, and as it will be explained later on, at 0 V the switching losses will increase drastically. This phenomenon is common in SiC technologies [2] and can be avoided by reducing the V_{GS} to for instance −5 V.

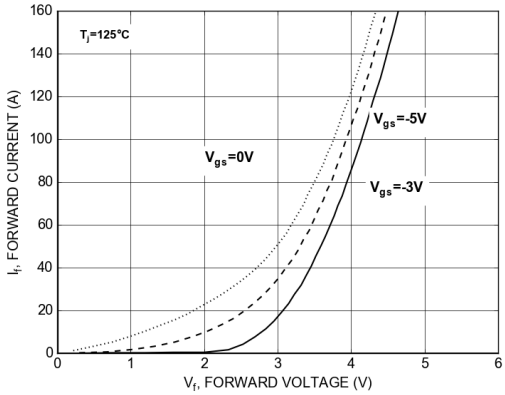

Figure 8. V_f vs. I_f for Different V_{GS} in a 20 mΩ, 1200 V SiC MOSFET Module

V_{TH}, Temperature Dependency

During previous chapters, the drift in the V_{TH} has been presented, when both a positive or negative gate bias is applied. An additional factor that influences the V_{TH} is the temperature. Like all MOSFETs, **onsemi** M 1 1200 V SiC MOSFETs, have a negative temperature coefficient. The consequence is that the V_{TH} could be reduced from a typical value around 2.6 V at 25°C to as low as 1.8 V at 175°C. Figure 9 shows typical V_{TH} values at different temperatures for a 40 mΩ device. This has to be considered when designing the gate driver circuit to avoid unwanted parasitic turn on. Once again, the data should be considered at the real application temperature. For instance, a 2 V voltage spike at the gate at room temperature is less likely to trigger a parasitic turn on than at 125°C.

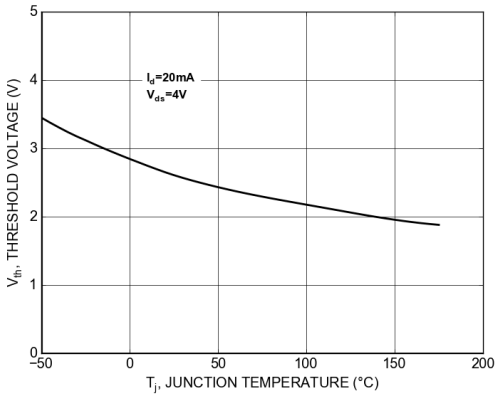

Figure 9. Typical VTH Values vs. Temperature in a 40 Ωm, 1200 V SiC MOSFET

In order to keep a safety margin in topologies sensitive to parasitic turn on, like a half−bridge. It is recommended to set a negative V_{GS} when the device is turned off.

DYNAMIC CHARACTERISTICS

For the characterization of the dynamic characteristics of **onsemi** M 1 SiC MOSFETs, a 20 mΩ half−bridge module using two 40 mΩ devices in paralleled has been used. Figure 10 illustrate the test set−up.

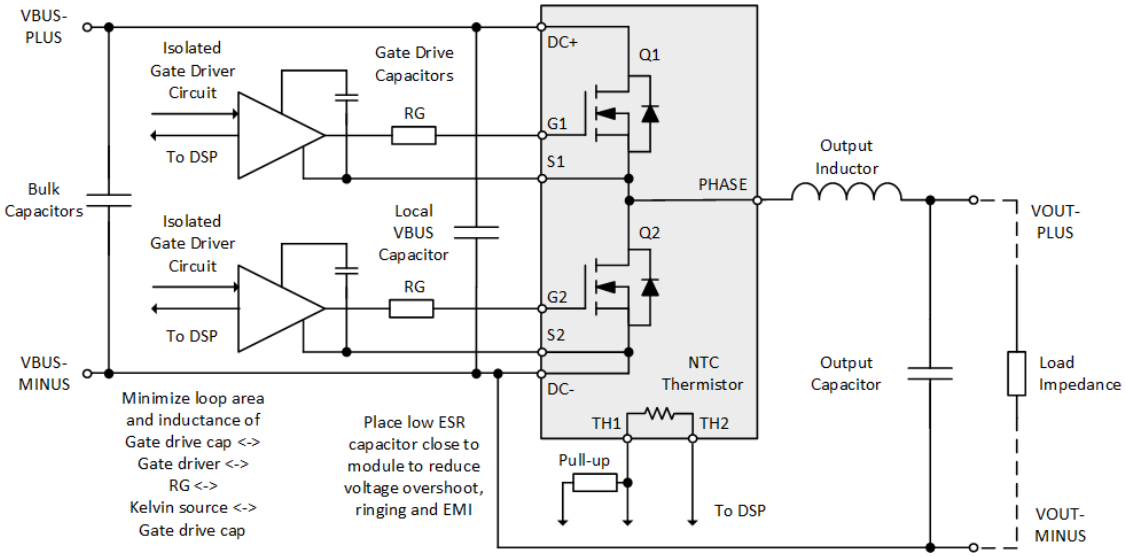

Figure 10. Block Diagram of Test Setup for the Dynamic Characterization

Figure 11 shows the turn on waveform of the mentioned test device. The magenta curve is the drain voltage of the low side MOSFET. The green curve is the current through the low side MOSFET.

The switching sequence starts when the gate driver is switched to 18 V at time t = 0. After an initial ramp up, the gate drive current starts off high and reduces as the gate voltage increases. The gate voltage rises until the threshold voltage is reached. The current increases until it reaches the current flowing through the diode: the load current + reverse recovery current + capacitive current.

The plateau voltage for a SiC MOSFET is highly dependent on load current. In Figure 11, the plateau voltage is approximately 10 V. The VGS for a given ID is given by the following equation.

$$iD = k(VGS - VT)^2$$

So the slope will vary with time as follows:

$$\frac{diD}{dt} = 2k(vGS - VT) \cdot \frac{d(vGS - VT)}{dt}$$

As the gate voltage changes approximately linearly with time, di/dt changes linearly with time. The voltage drop on Vds caused by L di/dt linearly decreasing with time starts from when the current reaches the threshold voltage and finishes when the current peak is reached.

The gate current and voltage reaches the plateau voltage. The gate current charges up the QGD and the drain voltage decreases to almost zero.

The drain current falls towards the load current with some ringing.

Finally, the gate voltage rises up to 18 V. The drain voltage reduces to the load current times $R_{DS(ON)}$ at 18 V.

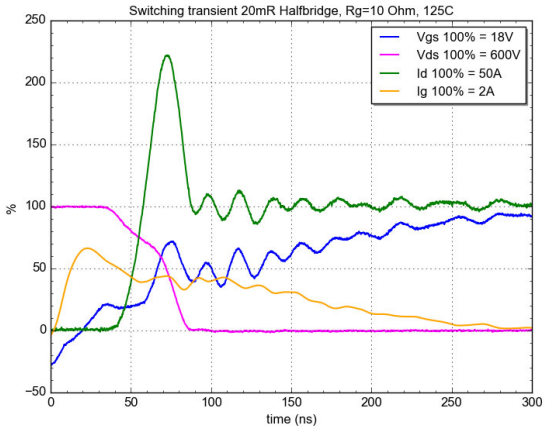

Figure 11. Turn On Waveform for 20 mohm, 1200 V Half Bridge Module

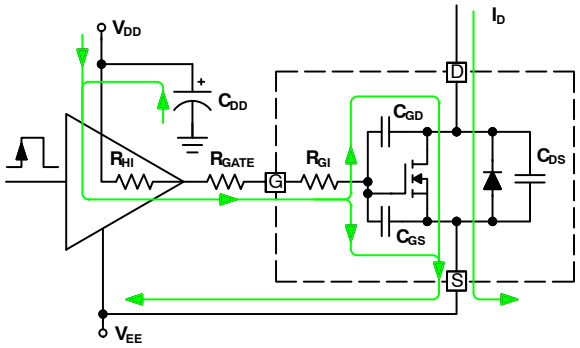

Figure 12. SiC MOSFET Source Current

Figure 13 shows the switch off waveform for a 20 mohm, 1200 V half−bridge module using two 40 mohm devices.

The switching sequence starts when the gate driver is switched to −5 V at time t = 0. After an initial ramp up, the gate drive sink current starts off high and reduces as the gate voltage increases. The gate voltage falls until the plateau voltage is reached. The plateau is lower than during turn ON as there is no reverse recovery current. The voltage rises as the QGD is discharged. Some of the drain current is used to discharge the non−linear COSS capacitance which shows up as a negative slope in the drain current.

The gate voltage overshoot is caused by the loop inductance in the circuit: nearest capacitor to the DC bus – DC + contact of module – DC − contact of module – back to the DC bus capacitor. The connection between the module and the capacitor should be made as low inductance as possible to minimize the ringing voltage.

When the peak voltage is reached, the gate driver discharges the gate from the plateau voltage to the threshold voltage, bringing the current down to zero. The gate driver continues to discharge the gate until it reaches −5 V.

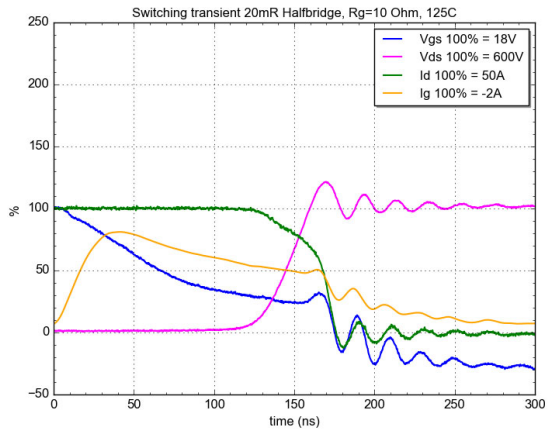

Figure 13. Turn OFF Waveform for 20 mohm, 1200 V Half Bridge Module

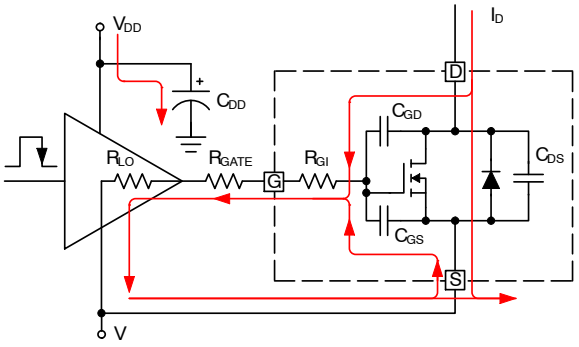

Figure 14. SiC MOSFET Sink Current

Switching Losses Scaling with Temperature

Just like in the static characteristics, the temperature at which the SiC MOSFET operates will have an impact in the switching performance. However, as it can be observed in Figure 15, E_{ON} and E_{OFF} show nearly a flat temperature coefficient and the switching performance at 150°C will be very close to the characteristics at 25°C. This is however not the case for the reverse recovery losses (E_{rr}), which are negligible at 25°C, but as the temperature increases, they might reach a point in which they should be considered in the loss calculation. For these reasons as already explained in the previous chapter, it is crucial to consider any parameter at the real working temperature and not just at 25°C.

In case of the E_{rr} it is worth noticing that according to Lutz et. al [3] a significant portion of these losses are capacitive and not pn junction losses. These capacitive losses will look like losses on an oscilloscope but will not cause heating in the body diode. The effect of these losses and magnitude are dependent on voltage and current, but could represent as much as 40% of the E_{rr} losses shown in a typical datasheet. That is why, taking directly the E_{rr} losses from the datasheet is a conservative approach. The overall losses can then only be measured by comparing the system input power and the system output power in the real application.

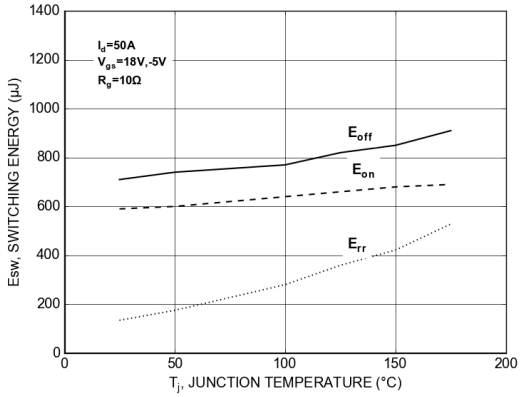

Figure 15. Switching Losses vs. Tj in a 20 mΩ, 1200 V SiC MOSFET Module

Switching Losses Scaling with Drain Current (I_D)

The switching losses of any MOSFET are by definition the result of the time integral of voltage multiplied by the current during any of the switching event.

$$E_{SW} = \int_0^t V_{DS}(t) \cdot I_D(t)dt$$

Therefore, it is to be expected that the losses increase as the current increases. However, comparing the behavior of M 1 1200 V SiC MOSFETs to an IGBT there are some differences. As it can be observed in Figure 16, the behavior of E_{ON} versus I_D for a 20 mΩ, 1200 V SiC module in half−bridge configuration is linear, these losses will depend on the recovery of the corresponding diode in the commutation loop. The recovery losses of the body diode also behave in a linear mode. On the other hand, the E_{OFF} losses start with a quadratic increase until a certain point in which they also become linear.

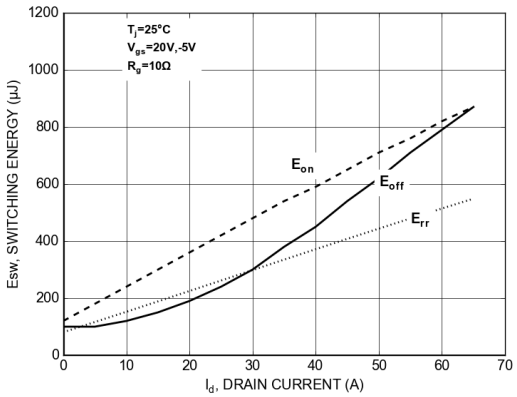

Figure 16. Switching Losses vs. I_D Characteristics in a 20 mΩ, 1200 V SiC MOSFET Module

Switching Losses vs. Drain Source Voltage (V_{DS})

Another direct factor in the switching losses is as explained in the previous point the V_{DS} in this case, as shown in Figure 17 the E_{ON} and E_{OFF} and E_{rr} behave in a linear manner although with a different slope.

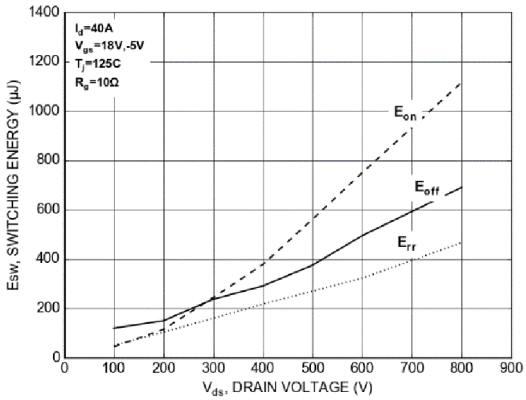

Figure 17. Switching Losses vs. V_{DS} in a 20 mΩ, 1200 V SiC MOSFET Module

Gate Resistance (R_G) Impact on the Switching Performance

The controllability of a switching device by external means is a key factor in the design of any circuit. In case of a MOSFET or an IGBT, despite being voltage−controlled devices, one of the most common ways to influence their switching behavior is to modify the external gate resistance R_G that, among other things, regulates how quickly the different capacitances involved in the switching event will be charged or discharged. Thus, directly influencing the switching times as well as di/dt or dv/dt.

In a first stage, the influence of the R_G on the losses needs to be considered when selecting the appropriate value. A higher R_G will slow down the device leading to higher E_{ON} and E_{OFF} losses. Figure 18 shows the behavior of the switching losses vs. R_G in a 20 mΩ, 1200 V SiC MOSFET module with M 1. The positive effect of a higher R_G is the decrease of the E_{rr} losses due to the smoother behavior of the MOSFET body diode at slower switching speeds.

However, this does not compensate the increase in the ON and OFF losses.

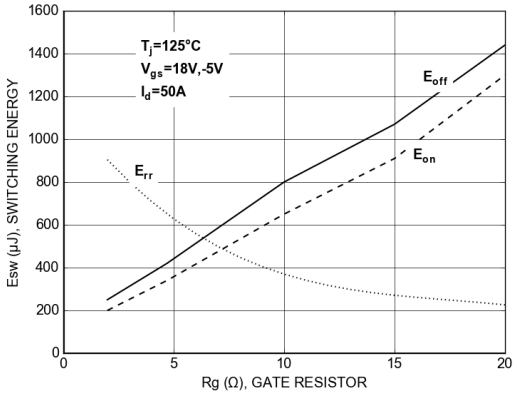

Figure 18. Switching Losses vs. R_G in a 20 mΩ, 1200 V SiC MOSFET Module

The obvious conclusion is to keep the R_G as low as possible. On the other hand, any circuit has parasitic inductances and capacitances that might lead to a critical voltage overshoot or oscillations that generate potential Electromagnetic Interferences (EMI) if a device is turned on too quickly, this does not only concern the main current commutation path, but also the gate circuit. On top of this, in some applications the dV/dt might be limited for safety reasons. For these reasons, it is important that the speed of the device can be easily adjustable with the R_G or eventually a gate capacitance (C_G), although the latter is not recommended as it could create severe oscillations in the gate. Figure 19 shows the influence that the R_G has on the dV/dt in a 1200 V, 20 mΩ half−bridge module using **onsemi** M 1 SiC MOSFETs. The graphic shows that the modification in the R_G enables the user to have a strong influence in the dV/dt, making it possible to adapt the switching behavior to the requirements of the circuit and the application. In this way, each user can easily find the best trade−off between switching losses and switching speed for their own application.

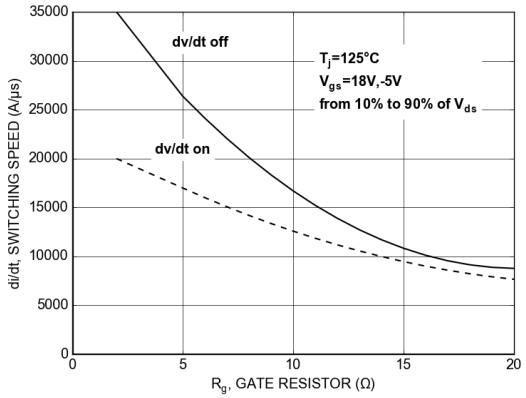

Figure 19. dV/dt Controllability with R_G in a 20 mΩ, 1200 V SiC MOSFET Module

Effect of V_{GS} on the Switching Losses

During the first chapters of this application note, the effects of the V_{GS} over the static characteristics of **onsemi** M 1 1200 V SiC MOSFETs were discussed. The conclusion was to use the device at least at + 18 V and that a higher voltage up to + 20 V could be beneficial. If the switching performance is now being considered, the conclusion will be the same. Figure 20 shows the dependency of the switching losses vs. V_{GS}. The E_{OFF} is independent of the positive V_{GS} : in the graph, the three E_{OFF} curves overlap. On the other hand, the V_{GS} will have a significant impact on the E_{ON} and E_{rr} behavior. If the V_{GS} is increased and the same R_G is used, the current charging the C_{GD} and C_{GS}. The consequence will be a faster switching of the device thus reducing the E_{ON} losses, this has the opposite effect on the E_{rr} as the increased speed will induce higher recovery losses in the body diode of the opposite MOSFET.

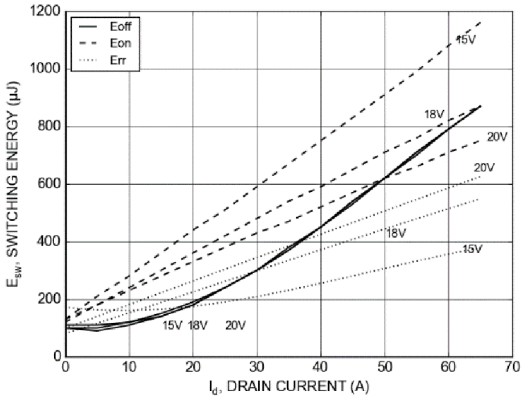

Figure 20. Influence of Positive V_{GS} over Switching Losses in a 20 mΩ, 1200 V SiC MOSFET Module

If the total losses are considered, like shown in Figure 21, the decrease in E_{ON} losses at higher V_{GS} overcompensates the increase in the E_{rr}, making it more efficient to switch the device at a higher V_{GS}. Of course other considerations such as EMI or dV/dt should be consider as well.

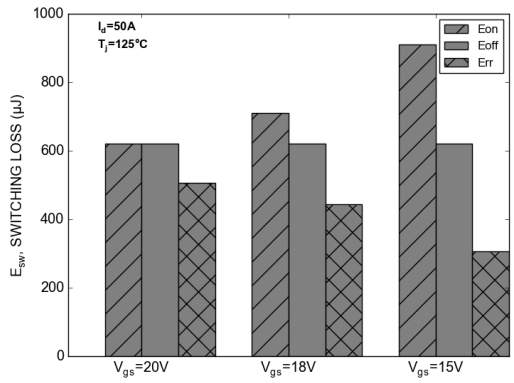

Figure 21. Total Losses for Different Positive V_{GS} in a 20 mΩ, 1200 V SiC MOSFET Module

Looking at the negative gate bias, previously it was highlighted the importance of using a negative voltage to fully close the channel during when the body diode is supposed to conduct. This will also have an impact on the switching losses. As it can be observed in Figure 22, while the negative gate voltage has nearly no impact on the E_{ON} or E_{rr} losses, the E_{OFF} losses can be drastically impacted. While the difference between – 5 V and −3 V is around 25%, if a 0 V negative gate bias is used, the E_{OFF} losses could double.

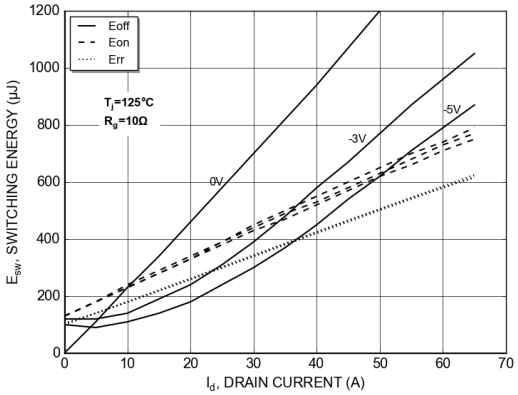

Figure 22. Influence of Negative V_{GS} over Switching Losses in a 20 mΩ, 1200 V SiC MOSFET Module

This effect can be also observed in Figure 23 where the total losses are shown.

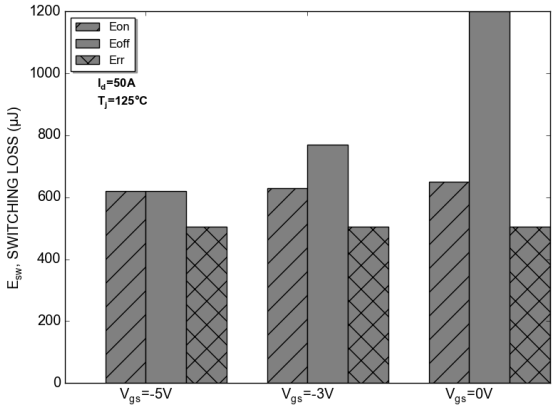

Figure 23. Total Losses for Different VGS in a 20 mΩ, 1200 V SiC MOSFET Module

Short Circuit with Stand Time (SCWT)

In some applications, the SCWT of a device is an important requirement during the selection process. This feature does not come without a penalty though. Having a longer SCWT will have an impact on the static and dynamic performance. That is why in many devices in order to achieve a better performance this feature is neglected.

In case of **onsemi** 1200 V M 1 SiC MOSFETs, a certain design margin has been left to provide short circuit withstand capability. The time that the device will be able to survive a short circuit will depend on many factors, the most important ones being the V_{DS} and the reference temperature at which the device might suffer the short circuit event. Like in many other parameters discussed in this application note, it is important to look at the characteristics at the right temperature, while the difference between 125°C and 150°C is not significant, the SCWT of the SiC MOSFET could be significantly better at 25°C. In order to provide relevant data for common operation temperatures, a starting temperature of 150°C has been selected for this document. Figure 24 shows the typical SCWT for different V_{DS}.

Important note: These are typical reference values and not guaranteed, please refer to datasheet values or contact your local technical support.

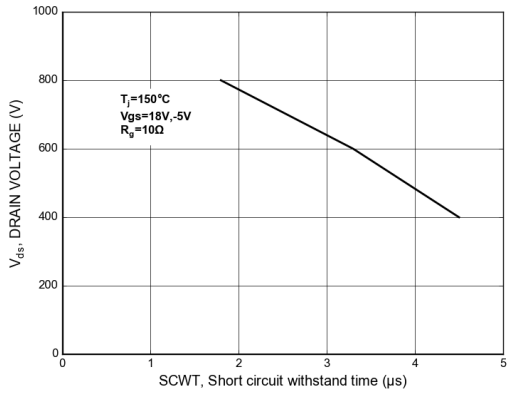

Figure 24. Short Circuit with Stand Time vs. V_{DS} in a 20 mΩ, 1200 V Half−bridge SiC MOSFET Module

Figure 25 shows the short circuit behavior of a real measurement in a 20 mΩ, 1200 V SiC MOSFET module at 150°C.

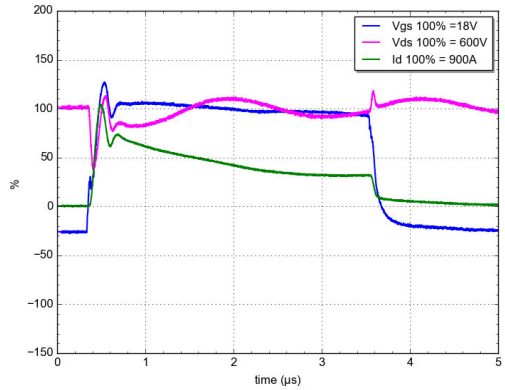

Figure 25. Short Circuit Behavior in a 20 mΩ, 1200 V Half−bridge SiC MOSFET Module

Dynamic Characteristics of the Body Diode

As mentioned in previous chapters, even if it is not recommended to use the body diode of the SiC MOSFET due to its high conduction losses, this cannot always be avoided. One possibility to improve the total losses was as mentioned to activate the channel of the MOSFET to improve the static behavior, this will however have little influence on the dynamic performance. An additional method would be to have an external SiC diode in parallel to the SiC MOSFET. However, in order to fully disable the body diode, this should be decoupled from the main commutation path as shown in Figure 26 for a half−bridge.

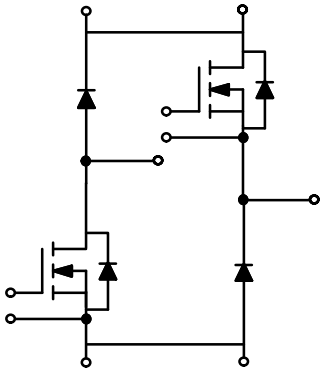

Figure 26. Half−bridge with Split Output

This split introduces not only the additional SiC diode, but also adds complexity in the layout. Comparing the dynamic behavior of the external SiC diode with the body diode, shown in Figure 27, it can be observed the external SiC diode does improve the reverse recovery behavior. This improvement could be marginal though; especially taking into account that part of the body diode losses are non−dissipative. Therefore, the user needs to consider whether it pays off to add this additional component with the corresponding increase in cost and complexity.

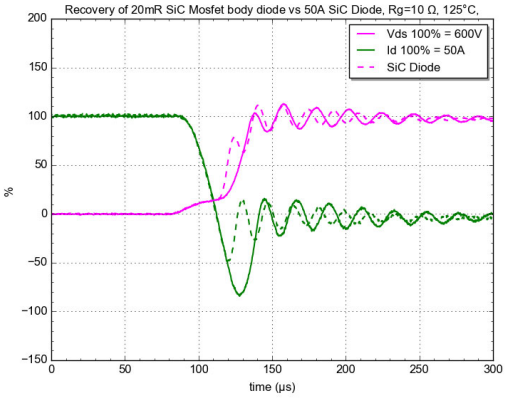

Figure 27. Recovery Behavior of an External SiC Diode (Dashed Line) vs. the Body Diode of the SiC MOSFET (Continuous Line)

Effects of Adding a Snubber Capacitor Inside the Power Module

The stray inductance in any design will play a key role in the switching performance of the device, not only in terms of efficiency, but also contributing to unwanted behaviors, such as ringing or high voltage overshoot. Considering that SiC devices are mainly used in fast switching applications, the risk to have unwanted effects of the stray inductance becomes even higher. That is why one of the first recommendations in any design is to keep the parasitic inductance as low as possible. Nevertheless, even the most experienced designer will not be able to avoid certain parasitic intrinsic to the package and a the minimum PCB rooting required.

Figure 28, shows the schematic of the main components in the critical switching loop in a standard half−bridge configuration. In order to reduce the length of the critical loop, a low ESR capacitor should be placed as close as possible to the module. However, this will not prevent from including in the loop the inductance of the pins, the PCB trace and the leads of the capacitor.

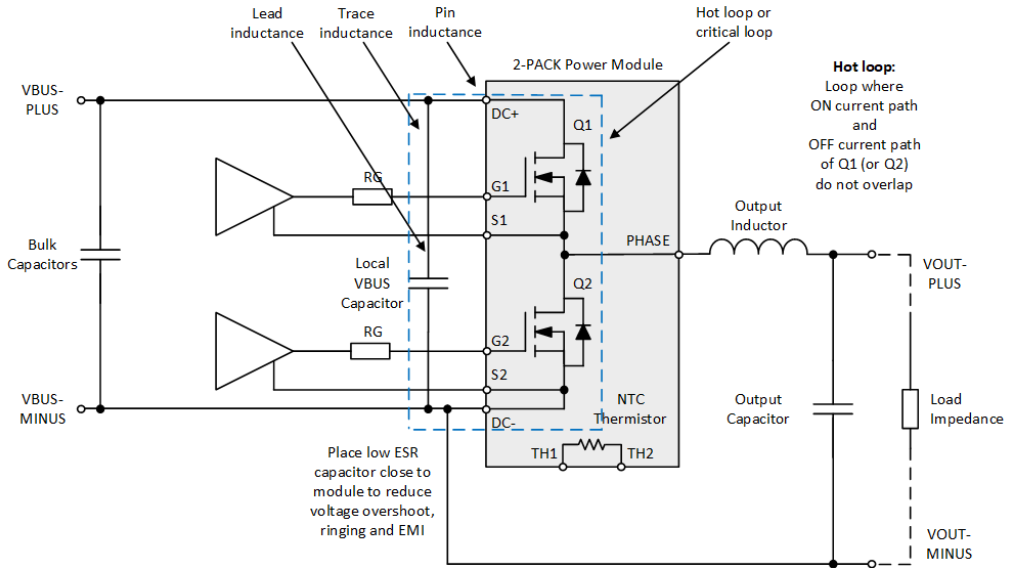

Figure 28. Schematics of a Half−bridge Module with External Capacitor

In order to reduce even more the length of the critical loop, an additional capacitor could be integrated inside to module. This is illustrated in Figure 29. In that way, we can reduce even further the parasitic inductance by eliminating to some extent the effects of the pin, trace and lead inductances. The size of the integrated capacitor is limited by the space available inside the module, for instance for this study a 100 nF capacitor has been used.

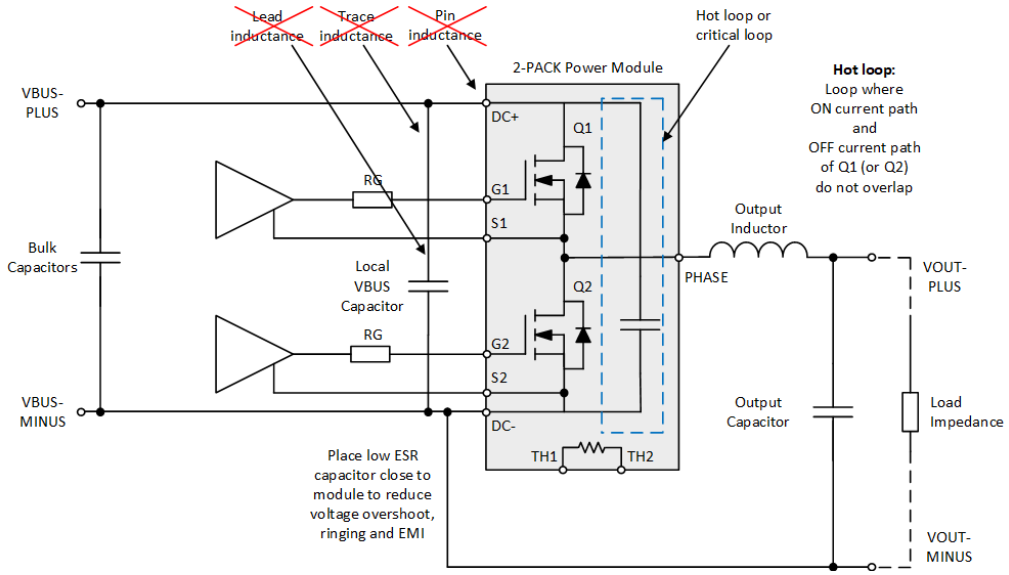

Figure 29. Schematics of a Half−bridge Module with Integrated Capacitor

The result of reducing the inductance of the critical loop will be an improvement on the switching behavior. In the first place, and as it can be seen in Figure 30, the voltage overshoot at turn−off can be reduced from nearly 150% to barely 120%.

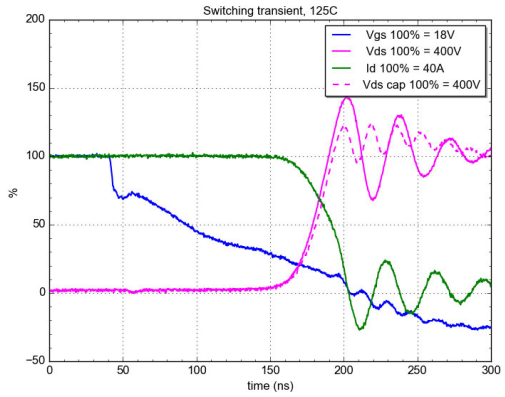

Figure 30. Turn−off Behavior of a Half−bridge with Integrated Versus External Capacitor

An immediate consequence of this reduced voltage overshoot will be a reduction in the Eoff losses as indicated in Figure 31. On the other hand as we increase the current, the Eon losses might increase. In any case, the total losses will see an improvement in the common current capability of the device.

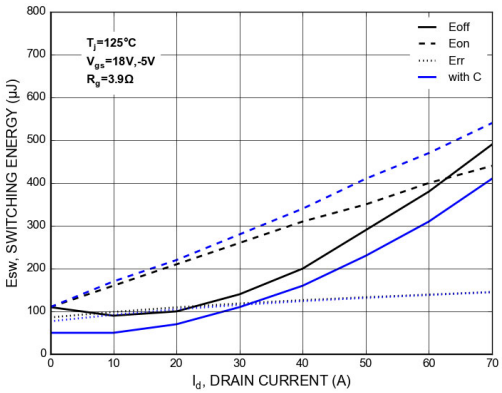

Figure 31. Switching Losses with and without Integrated Capacitor

NCP51705 SiC GATE DRIVER

The NCP51705 is a SiC gate driver that includes a high level of flexibility and integration making it fully compatible with any SiC MOSFET in the market. The NCP51705 top level block diagram, shown in Figure 32, includes many basic functions common to what might be expected from any general purpose gate driver, including:

1. V_{DD} positive supply voltage up to 28 V
2. High peak output current of 6 A source and 10 A sink
3. Internal 5 V reference made accessible for biasing 5 V, low−power loads up to 20 mA (digital isolator, opto−coupler, μC, etc)
4. Separate signal and power ground connections
5. Separate source and sink output pins
6. Internal thermal shutdown protection
7. Separate non−inverting and inverting TTL, PWM inputs

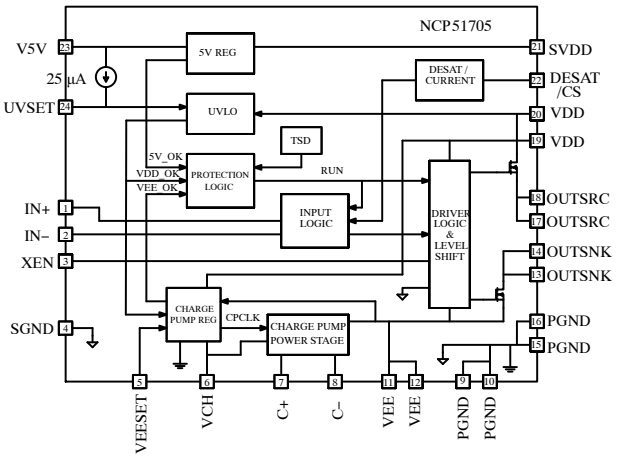

Figure 32. NCP51705 SiC Gate Driver Block Diagram

In addition, the NCP51705 is differentiated by several unique features (listed at the beginning of section Discrete SIC Gate Drive in TND6237/D) necessary for designing a reliable SiC MOSFET gate drive circuit using minimal external components. The advantages of the NCP51705 distinguishing features are detailed in the following section.

Over−Current Protection − DESAT

The implementation of the NCP51705 DESAT function can be realized using only two external components. As shown in Figure 33, the drain−source voltage of the SiC MOSFET, Q_1 is monitored via the DESAT pin through R_1 and D_1.

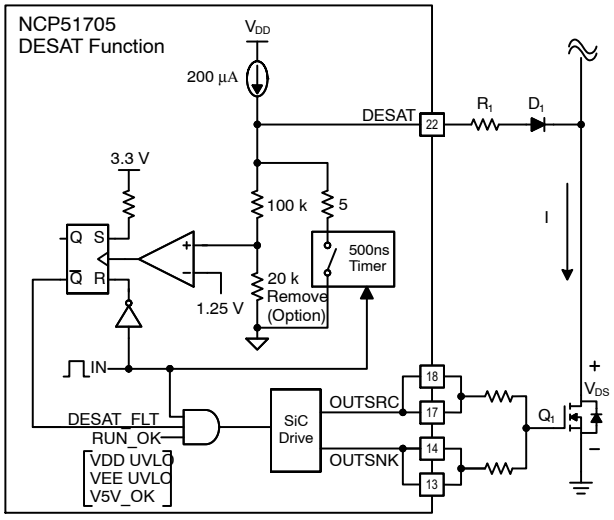

Figure 33. NCP51705 DESAT Function

During the time that Q_1 is off several hundred volts can appear across the drain−source terminals. Once Q_1 is turned on, the drain−source voltage rapidly falls and this transition from high−voltage to near zero voltage is expected to happen in less than a few hundred nano−seconds. During the turn−on transition, the leading edge of the DESAT signal is blanked by a 500−ns timer, consisting of a 5−Ω, low impedance pull−down resistance. This allows sufficient time for V_{DS} to fall while at the same time ensuring DESAT is not inadvertently activated. After 500 ns, the DESAT pin is released and the 200−μA current source provides a constant current through R_1, D_1 and the SiC MOSFET on−resistance. During the on−time, if the DESAT pin rises above 7.5 V, the DESAT comparator output goes HIGH which triggers the clock input of an RS latch. Such a fault will automatically terminate the trailing edge of the Q_NOT output on a cycle−by−cycle basis. The gate drive to the SiC MOSFET is thereby effectively reduced by an amount of time proportional to the de−saturation fault time.

The 200−μA current source is sufficient to ensure a predictable forward voltage drop across D_1 while also allowing the voltage drop across R_1 to be independent of V_{DS} during the on−time of the SiC MOSFET. If desired, DESAT protection can be disabled by connecting the DESAT pin to ground. Conversely, if the DESAT pin is left floating, or R_1 fails open, the 200−μA current source flowing through the 20−kΩ resistor, puts a constant 4 V on the non−inverting input of the DESAT comparator. This condition essentially disables the gate drive to the SiC

MOSFET. Some applications may prefer to sense the drain current using a current sense transformer and drive the DESAT pin externally. In this case the NCP51705 includes an IC metal option to remove the 20−kΩ resistor, allowing the DESAT pin to be used as a traditional pulse−by−pulse, over−current protection function.

The voltage on the DESAT pin, V_{DESAT}, is determined by equation (1) as:

$$V_{DESAT} = (200\ \mu A \times R_1) + V_{D1} + (I_D \times R_{DS}) \quad \text{(eq. 1)}$$

After assigning the maximum value for I_D (plus allowing any additional design margin) R_1 and I_D are selected such that $V_{DESAT} < 7.5$ V. Rearranging equation (1) and solving for R_1 gives:

$$R_1 = \frac{V_{DESAT} + V_D - (I_{D1} \times R_{DS})}{200\ \mu A} \quad \text{(eq. 2)}$$

In addition to setting the maximum allowable V_{DESAT} voltage, R_1 also serves the dual purpose of limiting the instantaneous current through the junction capacitance of D_1. Because the drain voltage on the SiC MOSFET sees extremely high dV/dt, the current through the p−n junction capacitance of D_1 can become very high if R_1 is not sized appropriately. Therefore, selecting a fast, high−voltage diode with lowest junction capacitance should be a priority. Typical values for R_1 will be near the range of 5 kΩ< R_1 < 10 kΩ but this can vary according to the I_D and R_{DS} parameters of the selected SiC MOSFET. If R_1 is much smaller than 5 kΩ, the instantaneous current into the DESAT pin can be hundreds of milliamps. Conversely, if R_1 is much larger than 10 kΩ, a RC delay ensues as a product of R_1 and the junction capacitance of D_1. The delay can be on the order of 100 μs, resulting in an additional delay time responding to a DESAT fault.

Charge Pump – V_{EE} (VEESET)

The NCP51705 operates from a single, positive supply voltage. Operating from a single V_{DD} supply voltage implies the negative V_{EE} voltage must be generated from the gate driver IC. The use of a switched capacitor charge pump is a natural choice for producing the required negative V_{EE} voltage rail. There are many different options for architecting a charge pump. The main challenges are maintaining accurate voltage regulation during transient conditions, switching at a frequency to decrease the size of capacitors and minimize external component count, thereby reducing cost and increasing reliability.

As can be seen from the charge pump functional block diagram shown in Figure 34, only three external capacitors are required to establish the negative V_{EE} voltage rail. The charge pump power stage essentially consists of two PMOS and two NMOS switches arranged in a bridge configuration.

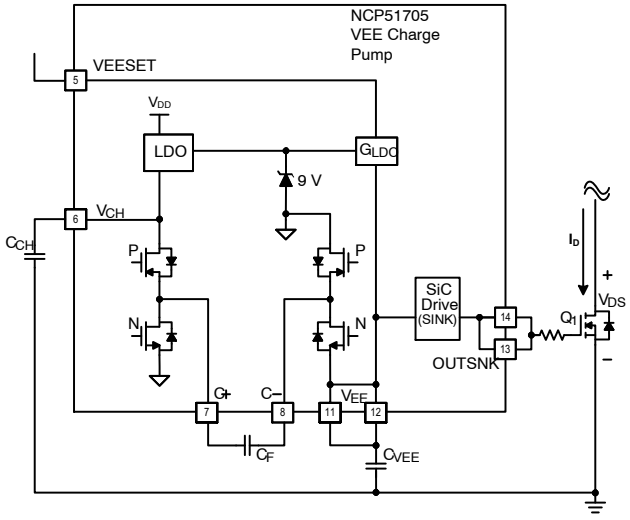

Figure 34. NCP51705 V_{EE} Charge Pump

An external flying capacitor, C_F, is connected between the midpoints of each leg of the bridge as shown. The switch timing is such that whenever the two upper PMOS devices are conducting simultaneously, V_{DD} appears across C_F. Similarly whenever, the two lower NMOS devices are conducting simultaneously, $-V_{EE}$ appears across C_F. The switching frequency is internally set at 390 kHz, with the two upper PMOS devices switching asynchronous with respect to the two lower NMOS devices. A 290 kHz, IC metal option is also available for applications desiring a lower charge pump switching frequency.

V_{EE} is regulated to the voltage set at V_{CH} which is determined by the internal low dropout regulator (LDO) voltage, programmable by VEESET. The voltage present at VEESET varies the gain (G_{LDO}) seen by the internal LDO. If VEESET is left floating (a 100−pF bypass capacitor from VEESET to SGND is recommended), then V_{EE} is set to regulate at −3 V. For a −5−V V_{EE} voltage, the VEESET pin should be connected directly to V5V (pin 23). If VEESET is connected to any voltage between 9 V and V_{DD}, then V_{EE} is clamped and set to regulate at the minimum charge pump voltage of −8 V. The charge pump starts when $V_{DD} > 7.5$ V and the V_{EE} voltage rail includes an internally fixed UVLO set to 80% of the programmed V_{EE} value. Since V_{DD} and V_{EE} are each monitored by independent UVLO circuits, the NCP51705 is smart enough to realize when both voltage rails are within limits deemed safe for a given SiC MOSFET load.

Alternatively, 0 V < OUT < V_{DD} switching can be achieved by disabling the charge pump entirely. When VEESET is connected to SGND the charge pump is disabled. With the charge pump disabled and V_{EE} tied

directly to PGND, the output switches between 0 V < OUT < V_{DD}. It is important to note that whenever VEESET is tied to SGND, V_{EE} must be tied to PGND. During this mode of operation the internal V_{EE} UVLO function is also disabled accordingly.

Another possible configuration is to disable the charge pump but allow the use of an external negative V_{EE} voltage rail. This option permits $-V_{EE}$ < OUT < V_{DD} switching with a slight savings in IC power dissipation, since the charge pump is not switching. With VEESET connected to SGND, an external negative voltage rail can be connected directly between V_{EE} and PGND. A word of caution, since VEESET is 0 V, the internal V_{EE} UVLO is disabled and therefore the NCP51705 is unaware if the V_{EE} voltage level is within the expected range.

This simple VEESET adjustment enables the highest degree of flexibility using the fewest external components while meeting the broadest range of SiC MOSFET voltage requirements. For convenience, the configurability of VEESET is summarized in Table 2.

Table 2. SEMICONDUCTOR MATERIAL PROPERTIES

VEESET	COMMENT	V_{EE}	V_{EE} (UVLO)
V_{DD}	9 V < VEESET < V_{DD}	−8 V	−6.4 V
V5V		−5 V	−4 V
OPEN	Add $C_{VEE} \leq 100$ pF from VEESET to SGND	−3 V	−2.4 V
GND	Remove C_{VEE} and connect V_{EE} to PGND	0 V	NA
GND	Connect V_{EE} to external negative voltage supply	$-V_{EXT}$	NA

Programmable Under Voltage Lockout − UVSET

UVLO for a gate driver IC is important for protecting the MOSFET by disabling the output until V_{DD} is above a known threshold. This not only protects the load but verifies to the controller that the applied V_{DD} voltage is above the turn−on threshold. Because of the low g_m value associated with SiC MOSFETs, the optimal UVLO turn−on threshold is not a “one size fits all.” Allowing the driver output to switch at low V_{DD} can be detrimental for one SiC MOSFET but may be acceptable for another depending on heat−sinking, cooling and V_{DD} start−up time. The optimal UVLO turn−on threshold can also vary depending on how the V_{DD} voltage rail is derived. Some power systems may have a dedicated, housekeeping, bias supply while others might rely on a V_{DD} bootstrapping technique similar to Figure 36.

The NCP51705 addresses this need through a programmable UVLO turn−on threshold that can be set with a single resistor between UVSET and SGND. As shown in Figure 35, the UVSET pin is internally driven by a 25−μA current source with a series gain of 6.

The UVSET resistor, R_{UVSET}, is chosen according to a desired UVLO turn−on voltage, V_{ON}, as defined in equation (3).

$$R_{UVSET} = \frac{V_{ON}}{6 \times 25\ \mu A} \qquad \text{(eq. 3)}$$

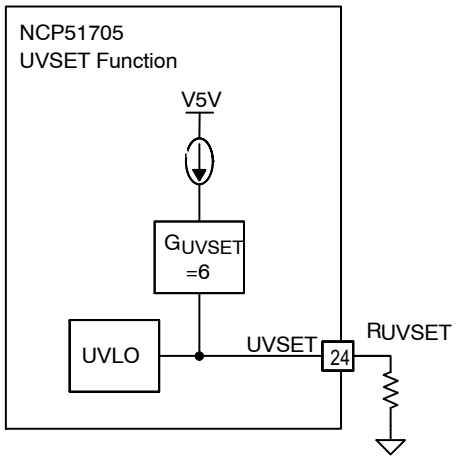

Figure 35. NCP51705 UVSET Programmable UVLO

The value for V_{ON} is typically determined from the SiC MOSFET output characteristic curves, such as those highlighted in Figure 1 from TND6237/D. Because the on−resistance of a SiC MOSFET dramatically increases even for a slight decrease in V_{GS}, the allowable UVLO hysteresis must be small. For this reason, the NCP51705 has a fixed 1−V hysteresis so that the turn−off voltage, V_{OFF}, is always 1 V less than the set V_{ON}.

For power supplies that include a dedicated housekeeping bias supply, V_{DD} is assumed to be above the desired V_{ON} threshold before the power system initiates soft−start or restart due to a fault recovery. For such systems, having a 1−V UVLO hysteresis is desirable and should not have any impact due to start−up considerations. However, some power systems start from a high−voltage and then rely on V_{DD} from a bootstrap winding as shown in Figure 36.

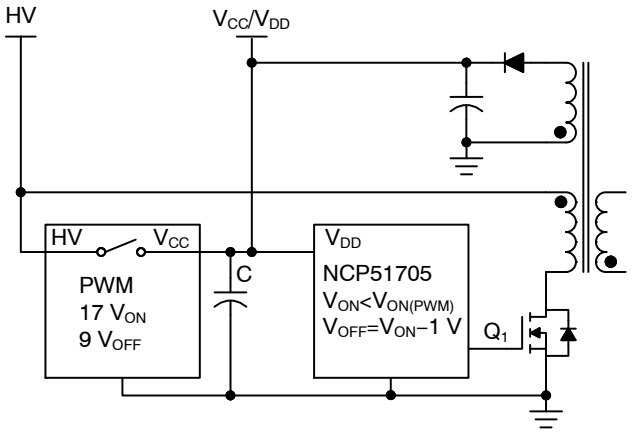

Figure 36. PWM Bootstrap Start−Up Example

A PWM controller with high−voltage (HV) start−up capability and fixed UVLO thresholds of V_{ON} = 17 V and V_{OFF} = 9 V is shown. As HV is applied, the internal pass switch opens when HV = V_{ON} = 17 V and the PWM controller draws start−up current from C_{VCC}. During this time, C_{VCC} is discharging and Q_1 must begin switching to build up voltage in the transformer bootstrap winding. This imposes a restriction on the allowable V_{ON} that can be programmed from R_{UVSET}. UVSET must be set to a value less than the UVLO V_{ON} of the PWM controller. These start−up details are further illustrated in Figure 37 where the PWM voltage thresholds are shown in blue and the NCP51705 in red.

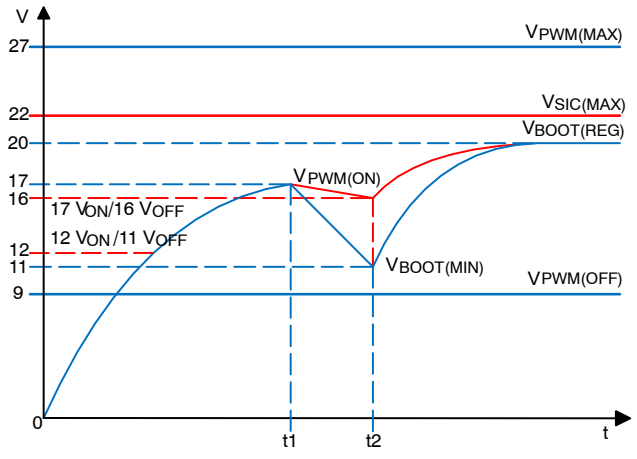

Figure 37. Bootstrap Start−Up Timing

For the purpose of switching the SiC MOSFET with the highest possible V_{GS}, it is desired to set V_{ON} as close to the UVLO turn−on of the PWM controller as possible. The trade off in doing so means ΔV = 1 V during Δt (t_2−t_1). The discharge of C_{VCC} is very shallow so a large capacitor value is required. For example, assuming the start−up current to be 1 mA, Δt = 3 ms and ΔV = 1 V, a 3−μF capacitor for C_{VCC} is required. Conversely, if V_{ON} is set to 1 V above the minimum bootstrap discharge voltage, $V_{BOOT(MIN)}$, C_{VCC} is allowed to discharge over a wider ΔV (17 V − 11 V) and a much smaller capacitor value can be used. Given the same 1 mA, Δt = 3 ms and allowing ΔV = 6 V, the required C_{VCC} capacitor value is reduced to 500 nF; a reduction by a factor of 6. However, the incurred penalty can be quite severe as the SiC MOSFET will be switching with V_{GS} = 11 V. Clearly, having the NCP51705 biased prior to start−up is the preferred approach.

Digital Synchronization and Fault Reporting − XEN

The XEN signal is a 5 V digital representation of the inverse of V_{GS}. For the purpose of reporting driver "status", it is considered more accurate that the PWM input since it is derived from the SiC gate voltage, propagation delays are greatly decreased. The intent of this signal is that it can be used in half−bridge power topologies as a fault flag and synchronization signal as the basis for implementing cross conduction (overlap) protection. Whenever XEN is HIGH, V_{GS} is LOW and the SiC MOSFET is OFF. Therefore if XEN and the PWM input signal are both HIGH, a fault condition is detected and can be digitally assigned to take whatever precautions might be desired.

Packaging

WBG semiconductors have enabled high−voltage converters to operate much closer to low−voltage (less than 100 V) switching frequencies. For low−voltage converters, the evolution of semiconductor packaging played a key role toward the modern achievement of switching performance seen today. Dual−sided cooling, clip bonding, thermally enhanced power packages and lower inductance, leadless packages are a few examples of silicon MOSFET packaging advancements. Similarly, the size of gate driver IC packages has undergone a tremendous size reduction. Shorter die to lead, bond wire connections combined with molded leadless packages (MLP) have been essential for minimizing parasitic inductance from the driver side. The co−packaging of the driver and MOSFET (DrMOS) is the latest step toward reducing parasitic inductance, raising efficiency and reducing board area. Advancements such as DrMOS are achievable because of the comparable low−voltages involved.

In the high−voltage converter realm, minimum spacing requirements such as creepage and clearance have left high performance SiC MOSFETs stuck in low−performance TO−220 and TO−247 type packages. These packages are well established and have long been an industry standard. They are well suited for industrial applications, robust and easy to heat sink but have higher parasitic inductance due to their long leads and internal bond wires. SiC MOSFETs have now subjected these parasitic inductances to thermal stresses, frequencies and dV/dt rates never before envisioned with high−voltage, silicon transistors. Suffice to say, SiC is providing the stimulus for rethinking high−voltage discrete packaging.

Although not the case with discrete components, a SiC gate driver is able to take full advantage of the same packaging advancements used with drivers intended for low−voltage converters. The NCP5170 die is packaged into a 24 pin, 4 × 4 mm, thermally−enhanced MLP as shown in Figure 38.

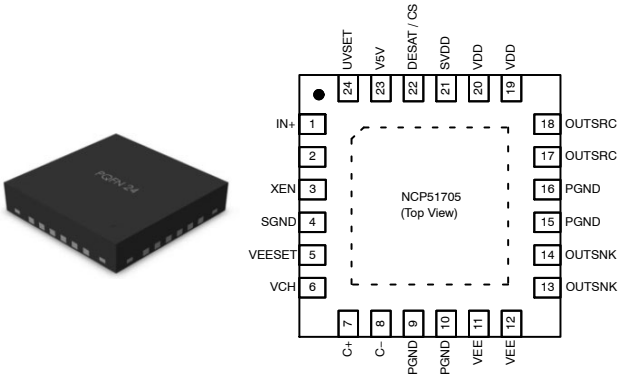

Figure 38. NCP51705 24 pin, 4 × 4 mm, MLP Packaging and Pin Out

All the high−current, power pins are doubled and located on the right−half of the IC. In addition to doubling the pins, each doubled pin connects to the die through internal double bond wires for achieving the lowest possible inductance. All low−power, digital signals are single pins only and are located on the left−half of the IC, providing a convenient, direct interface to the PWM or digital controller.

The bottom of the NCP51705 package consists of an electrically isolated, thermally conductive, exposed pad. This pad is not connected to PGND or SGND but is intended to be connected through thermal vias to an isolated copper PCB land for heat−sinking.

If thermal dissipation becomes a concern, specific attention should be paid to four dominant power dissipation contributors:

1. OUTSRC and OUTSNK losses associated with driving the external SiC MOSFET. These are gate charge related losses proportional to switching frequency. Reducing switching frequency will decrease power dissipation
2. LDO between V_{DD} and V5V, capable of sourcing up to 20 mA. Do not load the V5V any more than biasing a digital isolator or optocoupler
3. LDO between V_{DD} and VCH which is part of the internal charge pump
4. Internal charge pump power switches which can be disabled and replaced with an external negative bias, as mentioned in section Charge Pump−V_{EE} (VEESET)

SYSTEM PERFORMANCE

For V_{DD} > 7 V, the quiescent current ramps up linearly until the set UVLO threshold is crossed. The blue trace shown in Figure 39, represents V_{DD} versus I_{DD} with no input applied (non−switching), $V_{DD(UVLO)}$ = 12 V and no load on the V5V regulator. For 7 V < V_{DD} < 22 V, I_{DD} was measured to be 0.6 mA < I_{DD} < 2.3 mA. The flat line across the middle is a ~1−mA increase in I_{DD} current when V_{DD} crosses the UVLO threshold.

The red trace represent the case where a 100 kHz, 50% pulsed input was applied to IN+ while the internal charge pump is disabled. A 4.99 Ω + 2.2 nF load was used which is the equivalent input for a typical SiC MOSFET. The external source and sink resistance was 3Ω.. For 12 V < V_{DD} < 22 V, I_{DD} was measured to be 3.7 mA < I_{DD} < 5.5 mA.

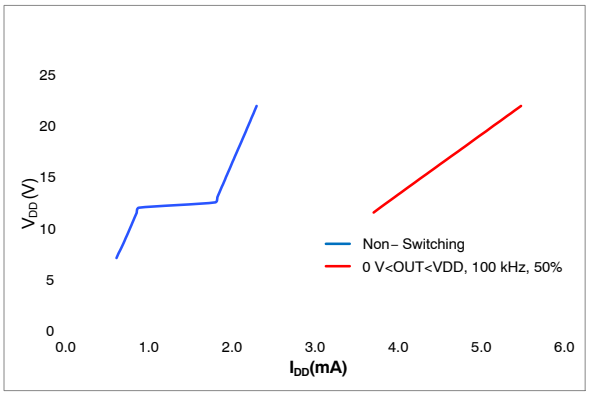

Figure 39. V_{DD} versus I_{DD}, Non−Switching versus Switching

The start−up waveform shown in Figure 40 shows IN + appearing prior to V_{DD}. V_{DD} is rising from 0 V to 20 V, with UVSET = 2 V (not shown) which equates to $V_{DD(UVLO)}$ = 12 V. V_{EE} is set to regulate at −5 V with VEESET = V5V (not shown) which equates to $V_{EE(UVLO)}$ = −4 V. The output is enabled when VEE = −4 V, even though V_{DD} > 12 V (V_{DD} = 15 V). Notice also that OUT (V_{GS}) is less than 20 V for almost 100 µs. Depending on the dV/dt rate of V_{DD} start−up, this time could be longer and therefore, the thermal stress to the SiC MOSFET should be taken into consideration when programming UVSET.

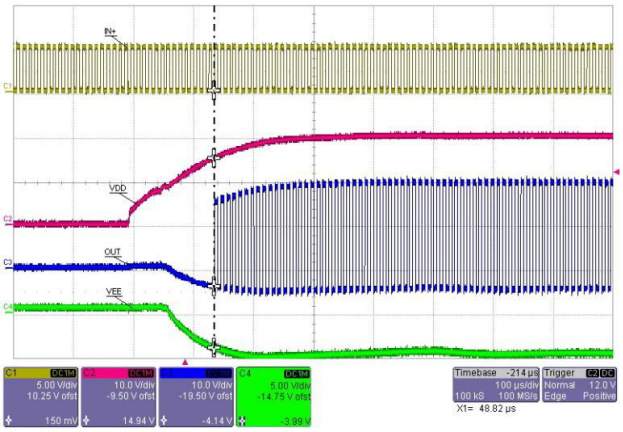

Figure 40. CH1−IN+, CH2−V_{DD}, CH3−OUT, CH4−V_{EE}; $V_{DD(UVLO)}$ = 12 V, $V_{EE(UVLO)}$ = −4 V

The same start−up waveform is shown in Figure 41 but UVSET = 3 V (not shown) which equates to $V_{DD(UVLO)}$ = 18 V. In this case, OUT (V_{GS}) is enabled when V_{DD} = 18 V, even though V_{EE} < −4 V (V_{EE} = −5 V). Which UVLO is dominant will depend on the dV/dt rate of V_{DD} versus V_{EE}. The key point is that the NCP51705 output is disabled until both, V_{DD} and V_{EE} are above and below their respective UVLO thresholds. Compared to Figure 40, notice the effect that a higher UVLO setting has on OUT (V_{GS}), where the first OUT pulse appears near 20 V and −5 V.

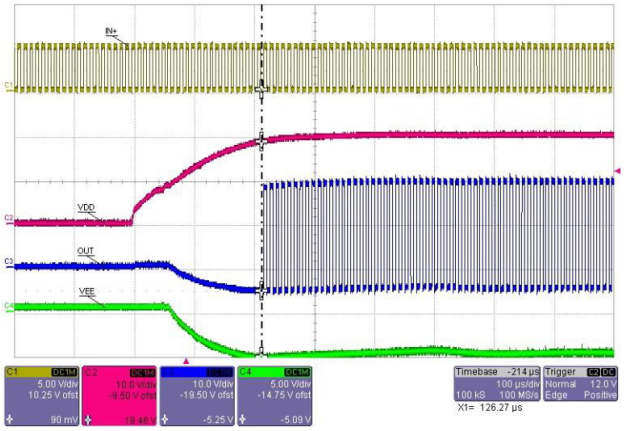

Figure 41. CH1−IN+, CH2−V_{DD}, CH3−OUT, CH4−V_{EE}; $V_{DD(UVLO)}$ = 18 V, $V_{EE(UVLO)}$ = −4 V

The NCP51705 internal charge pump has a slow control loop and the effect of this is seen by the slight undershoot and <400 μs correction observed during V_{EE} start−up shown in Figure 42. Beyond 400 μs, the V_{EE} voltage settles to the regulation set point of −3 V, −5 V or −8 V.

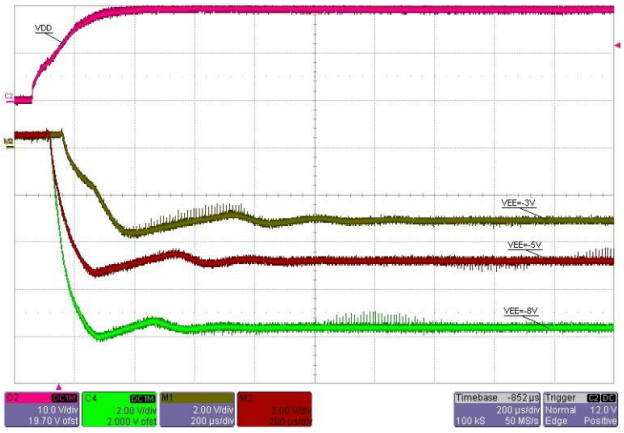

Figure 42. V_{EE} Start−Up

Shutdown operation is smooth with no glitches. As shown in Figure 43, OUT ceases switching and tracks V_{EE} which is unloaded. The discharge time from −5 V to 0 V for V_{EE} is approximately 300 ms.

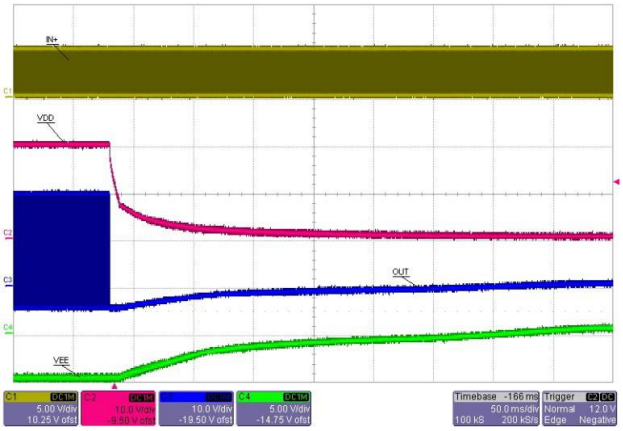

Figure 43. CH1−IN+, CH2−V_{DD}, CH3−OUT, CH4−V_{EE}; Shut−Down

A zoom of the time base from Figure 43 is shown in Figure 44. UVSET is configured for 3 V ($V_{DD(UVLO)}$ = 18 V) and the internal V_{DD} UVLO hysteresis is internally fixed at 1 V. The curser position reveals that V_{DD} = 17 V (18 V−1 V hysteresis), when the output is disabled, even though V_{EE} = −4.5 V (VEESET = V5V) and is still active according it's −4 V UVLO. Although the decay of V_{DD} is slow, a clean termination of the last output pulse can also be observed with no spurious pulses or glitches after UVLO_OFF.

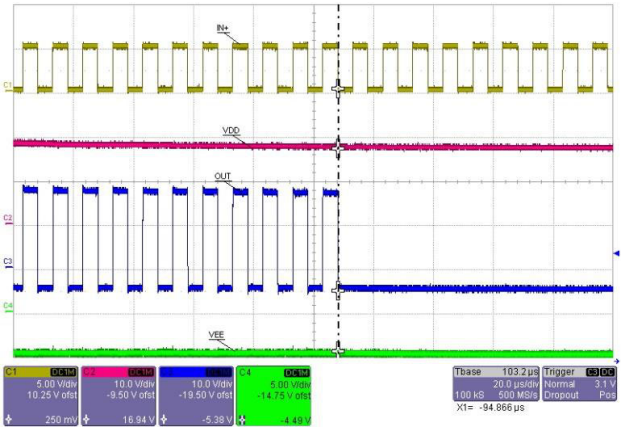

Figure 44. CH1−IN+, CH2−V_{DD}, CH3−OUT, CH4−V_{EE}; Shut−Down, V_{DD}_UVLO(OFF) = 17 V

The turn−on propagation delay is measured from 90% IN+ rising to 10% OUT rising. Although a SiC driver will operate at higher V_{DD}, most MOSFET propagation delays are specified switching into a 1−nF load with V_{DD} = 12 V.

Figure 45 shows the measured turn−on, propagation delay, under these standard test conditions, to be 19 ns.

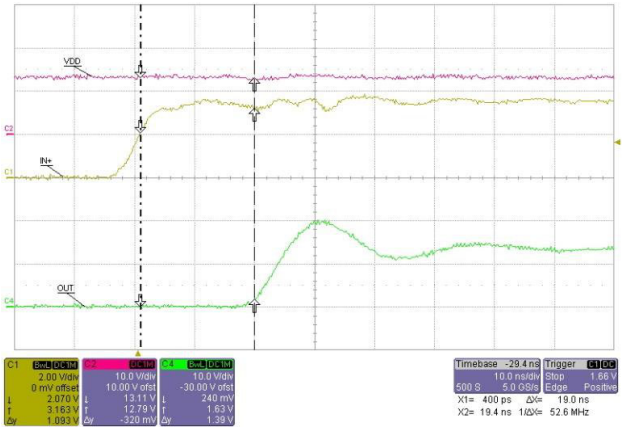

Figure 45. CH1−IN+, CH2−V_{DD}, CH4−OUT; Rising Edge Prop Delay

Similarly, the turn−off propagation delay is measured from 10% IN+ falling to 90% OUT falling. Figure 46 shows the measured turn−off, propagation delay under the same standard test conditions is 22 ns. The output rise and fall times for each edge are approximately 5 ns.

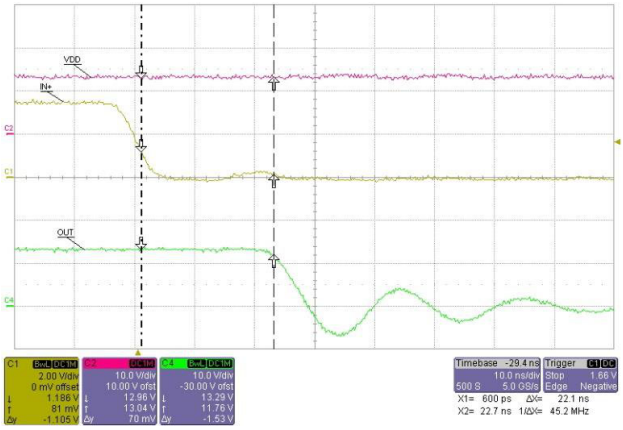

Figure 46. CH1−IN+, CH2−V_{DD}, CH4−OUT; Falling Edge Prop Delay

The DESAT and XEN waveforms are shown in Figure 47 and Figure 48 respectively. Since testing was done to verify IC validation only (no power stage), a 100−pF, fixed capacitor is connected to the DESAT pin. The waveforms shown in Figure 47 indicate DESAT is below the 7.5 V threshold and the output is switching under normal operation. If the IN+ frequency is decreased (increased on−time), the 100−pF DESAT capacitor will be allowed to charge to a higher voltage. This is shown in Figure 48 where the DESAT voltage has reached the 7.5−V threshold. The output trailing edge is terminated before the input voltage switches LOW. A shallow DESAT ramp is used to highlight the fact that no glitches appear on the terminated OUT pulse. In a switching power supply application, a small (<100 pF) external capacitor can be used on the DESAT pin for high−frequency noise filtering.

The XEN signal is the inverse of the OUT signal. Whether the driver is operating normal or under a DESAT fault, the XEN signal is shown to accurately track the inverse OUT signal for either case.

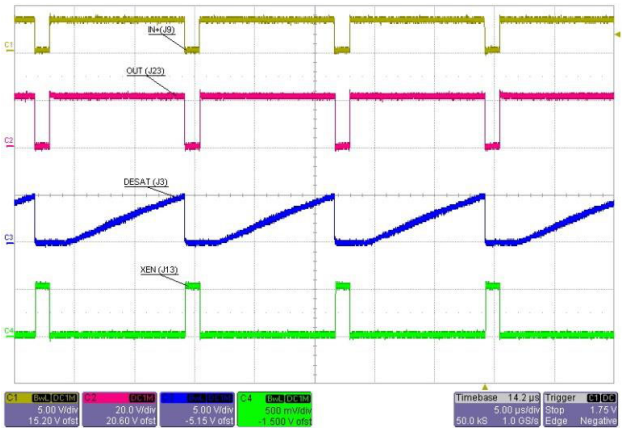

Figure 47. CH1−IN+, CH2−OUT, CH3−DESAT, CH4−XEN; V_{DESAT} < 7.5 V

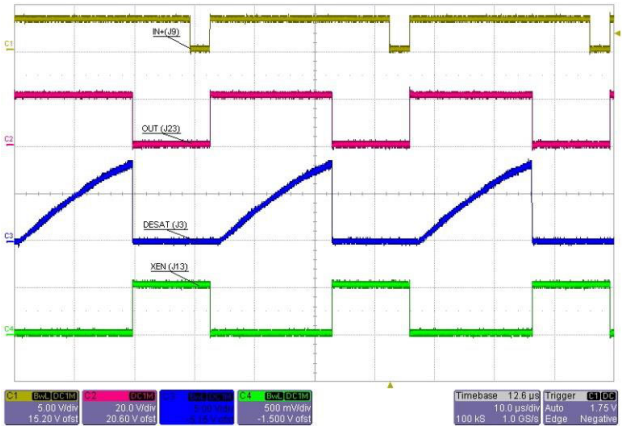

Figure 48. CH1−IN+, CH2−OUT, CH3−DESAT, CH4−XEN; V_{DESAT} = 7.5 V

APPLICATIONS

SiC MOSFETs can penetrate any application spaces where IGBTs are presently used. Some of the more common uses include high−voltage switching power supplies, hybrid and electric vehicle chargers, electric railway transportation, welders, lasers, industrial equipment and environments where high−temperature operation is critical. Two areas that are particularly interesting for SiC are solar inverters and high−voltage data centers. Higher dc voltages are beneficial for reducing wire gauge thickness, junction boxes, interconnections and ultimately minimizing conduction loss thereby increasing efficiency. Most large−scale, photovoltaic systems currently operate from a 1−kV dc bus and the trend is moving toward a 1.5−kV bus. Similarly, data centers using a 380−V distribution network can boost dc voltages as high as 800 V.

Several fundamental application examples highlighting the NCP5170 are shown as follows.

Low−Side Switching

Figure 49 shows a top level schematic highlighting the NCP51705 used in a low−side switching application. No isolation is shown so the interface between the controller and driver is direct, though this may not always be the case. This schematic is shown to raise awareness of how few external components are required to provide a fully functional, reliable and robust SiC gate drive circuit. It should also be mentioned that although only a single VDD voltage rail is required it should be rated for at least 50 V/ns to prevent spurious current pulses described in the discrete gate drive description in section Discrete SIC Gate Drive in TND6237/D. If the VDD voltage rail is provided by a dedicated auxiliary housekeeping power supply, special attention should be given to design a transformer featuring ultra−low, primary−secondary stray capacitance.

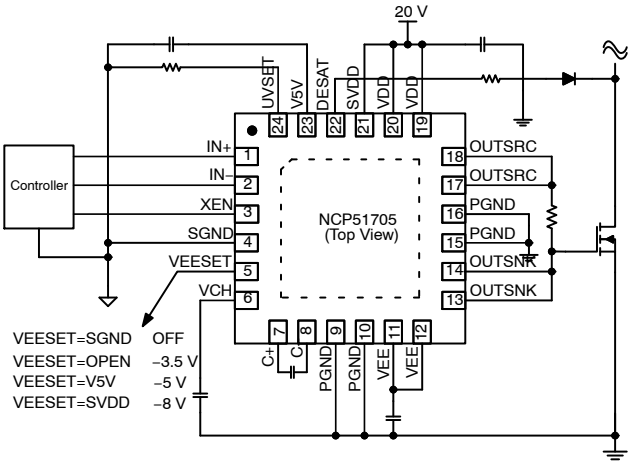

Figure 49. Low−Side Switching Example

Half−Bridge Concept

A more realistic use of SiC MOSFETs can be found in half−bridge power topologies such as the one shown in Figure 50. High power applications tend to prefer isolated drivers for both, the high−side and low−side. This implies the need for two digital isolators. Depending on the amount of IO crossing the isolation boundary, a strong debate for secondary−side control could be made for such applications. In this simplified example, IN+ and IN− (Enable) are the only two signals sourced from the digital controller and XEN is read back from the NCP51705. XEN is can be used as the timing information basis for developing gate drive timing, cross conduction prevention, dead−time adjustment and fault detection. In addition, temperature sensing, thermal management (fan control) and higher levels of fault response may also be done by the digital controller. The V5V from the NCP51705 can be used to power the secondary side of each digital isolator as shown Figure 50.

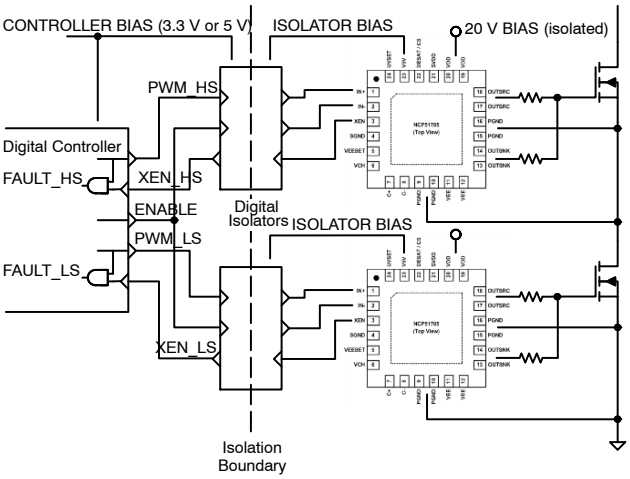

Figure 50. Half−Bride Concept

Quasi Resonant (QR) Flyback

A 100−W, QR flyback converter operating from a wide input range of 300 V < V_{IN} < 1 kV was designed using the NCP1340B1 controller and NCP51705 SiC driver. Converters of this class can typically be found in photovoltaic and industrial applications but when based on IGBT power stages, switching frequencies are in the range of 65 kHz. The schematic shown in Figure 51 is a QR flyback and the frequency is varying between 377 kHz < F_S < 430 kHz, from 100% to 25% load, at V_{IN} = 300 V.

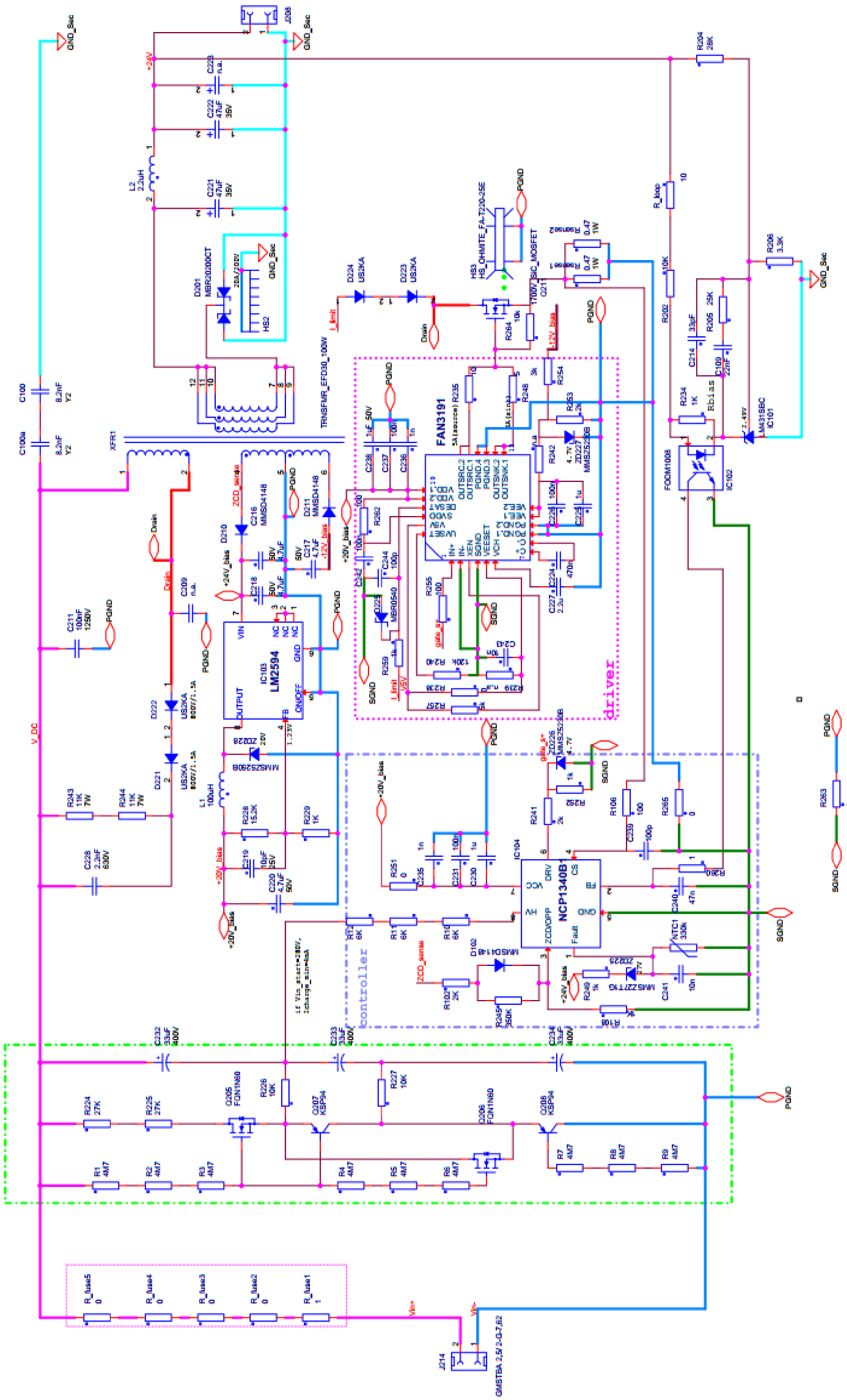

Figure 51. 1000 V to 24 V, 100 W, 400 kHz, QR Flyback

QR FLYBACK

For V_{IN} = 300 V, the drain−source voltage waveform is the sum of the input voltage and the reflected output voltage. The waveform shown in Figure 52 highlights the converter operating at full duty cycle operation (V_{IN} = 300 V) with 720 V appearing on drain−source of the SiC MOSFET. The V_{DS} rising transition is ~30 ns which equates to dV_{DS}/dt = 24 V/ns. The NCP1340B1, QR control enables a soft, resonant transition and valley switching (“near ZVS” turn−on at minimum V_{DS} resonance) on the V_{DS} falling edge and this is clearly visible on the blue waveform. Because the QR−flyback is a low−side only application and the falling dV_{DS}/dt edge is resonant, it may be possible for the SiC MOSFET to reliably switch between 0 V < V_{GS} < 20 V. Nonetheless, the design shown in Figure 51 opted for switching between −5 V < V_{GS} < 20 V resulting in more robust switching at the slight penalty of increased gate charge.

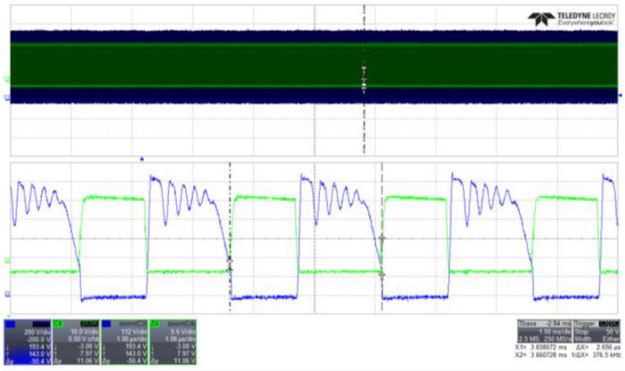

Figure 52. CH3 = V_{DS}, CH4 = V_{GS}; V_{IN} = 300 V, V_{OUT} = 24 V, I_{OUT} = 4 A, F_S = 377 kHz

General Purpose NCP5170 Customer EVB

A general purpose evaluation board (EVB) has been designed for the purpose of evaluating the NCP51705 performance in new or existing designs. The EVB does not include a power stage and is generic from the point of view that it is not dedicated to any particular topology. It can be used in any low−side or high−side power switching application. For bridge configurations two or more of these EVBs can be used at each SiC MOSFET in a totem pole type drive configuration. The EVB can be considered as an isolator + driver + TO−247 discrete module. The EVB schematic is shown in Figure 53.

The focus is to provide an ultra−compact design, where the leads of a TO−247 SiC MOSFET can be connected directly to the printed circuit board (PCB). Figure 54 shows simultaneous, top and bottom views of the EVB next to an adjacent TO−247 package for size scaling.

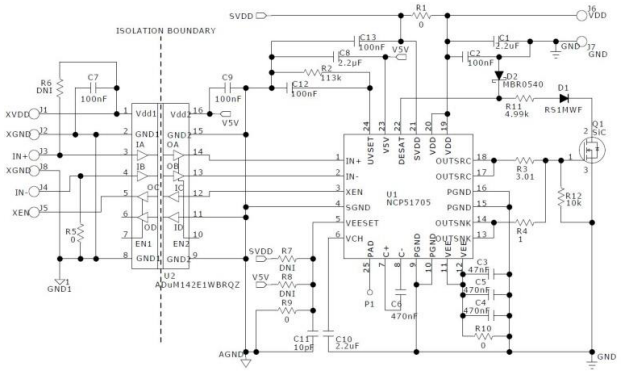

Figure 53. NCP5170 Mini EVB Schematic

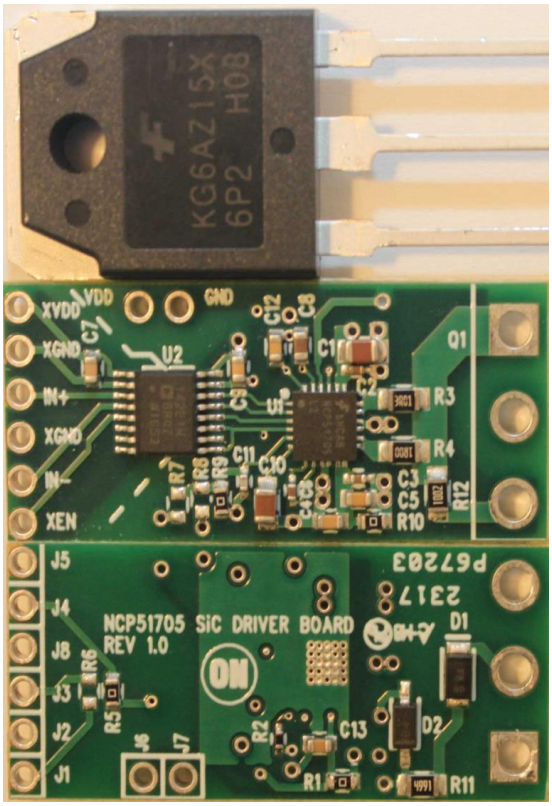

Figure 54. NCP5170 Mini EVB – Top View (35 mm x 15 mm)

When mounting into an existing power supply design and there is available PCB area in front of the TO−247, the EVB can be installed horizontally to the main power board, as shown in Figure 55. If possible, this should is the preferred mounting method.

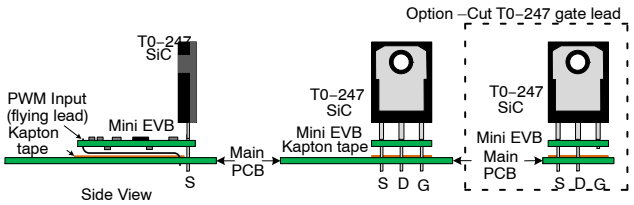

Figure 55. Horizontal EVB Installation

If large components on the main power board prevent horizontal installation, a second option is to install the EVB vertically so that it is parallel to the T0−247 package, or angled slightly away. Installing this way is less preferred due to the close proximity of the driver to the high dV/dt emitted from the TO−247 drain tab. In either case, the back tab of the TO−247 package remains exposed and can be attached to a heat−sink if necessary. Installation and operation details are available in the EVB User Guide.

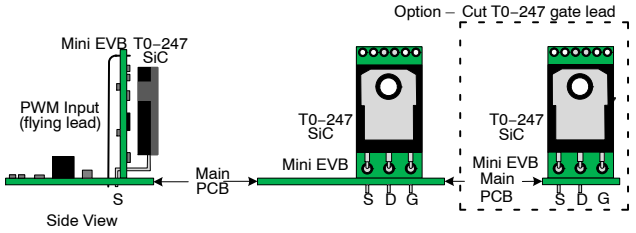

Figure 56. Vertical EVB Installation

The EVB comes initially configured to accept a PWM signal that is positive input logic (IN− connected to GND1). However, IN− can easily be used as an active enable or reconfigured for inverting input logic if desired. The driver output comes preconfigured for 0 V < V_{OUT} < V_{DD} switching. All the connections and resistor placeholders are available to reconfigure VEESET for −3 V, −5 V or −8 V V_{EE} switching. Finally, the UVSET option is preprogrammed for 17−V turn−on operation which is considered a safe level for SiC MOSFETs.

PARAMETRIC PERFORMANCE

MOSFETs and IGBTs are parametrically characterized using the well know double pulse test platform. The double pulse test method essentially applies two pulses to the gate−source of a low−side SiC MOSFET considered to be the device under test (DUT). The DUT is inserted into a socket connected to a clamped inductive switching circuit similar to the one shown in Figure 57.

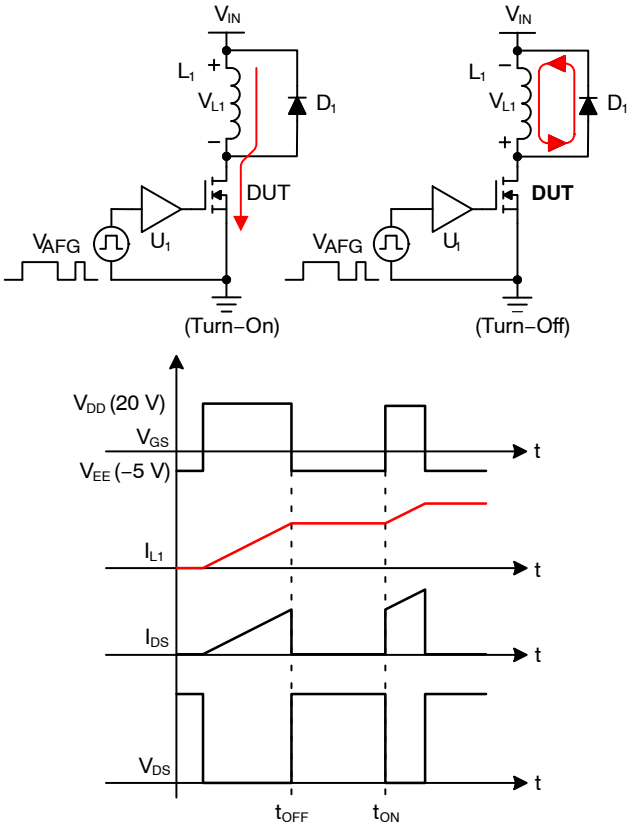

Figure 57. Double Pulse Test Circuit and Waveforms

The on−time of the first pulse is adjusted to achieve a desired peak drain−source current. The inductor is large and the off−time is short enough such that I_{L1} remains nearly constant during the off−time, freewheeling period. As a result, a second, shorter pulse is applied with the same amplitude of drain−source current. This test method allows precise control of I_D and V_{DS} necessary for establishing dynamic switching, parametric performance as well as benchmarking one device against another.

The double pulse test method can also be used to characterize gate driver performance. Leaving the SiC, DUT fixed, various gate drive circuits can be characterized as U_1 becomes the new "DUT." dV/dt and dI/dt switching performance is compared between the NCP5170 EVB shown in Figure 53 and Figure 54 and the simple optocoupler gate drive circuit shown in Figure 58.

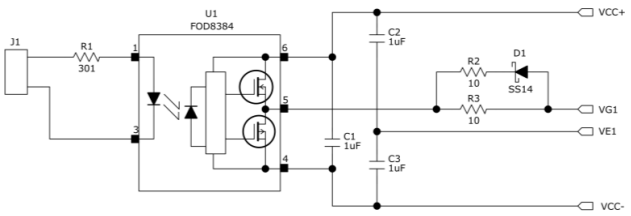

Figure 58. FOD8384 SiC Opto Gate Drive Circuit

The FOD8384 optocoupler driver is capable of withstanding V_{DD} bias up to 30 V, making it well suited for −5 V < V_{GS} < 20 V switching. Similar to the example shown in Figure 58, the FOD8384 driver is not a complete SiC MOSFET gate drive circuit. Therefore, since features between the two circuits are not comparable, test results and comparisons are limited to dynamic switching only.

The rising and falling VGS waveforms for both circuits are show for comparison in Figure 59 and Figure 60 respectively. Both circuits are using 1 Ω source and sink gate resistors. These gate drive edges are shown driving a 1.2 kV, SiC MOSFET with 600 V present on V_{DS} and 30 A flowing through I_D. The NCP51705, V_{GS} rising edge appears as purely resistive from −5 V < V_{GS} < 10 V and then capacitive *RC* charging from 10 V < V_{GS} < 20 V. This is indicative of the NCP51705, 6 A_{PK} sourcing current compared to the 1 A_{PK} sourcing current from the FOD8384. As a result the NCP51705 has a V_{GS} rise time of 37.5 ns, compared to 57.6 ns for the FOD8384 switching under the same test conditions. Similarly, the V_{GS} fall time for the NCP51705 is 25.2 ns, compared to 34.5 ns for the FOD8384.

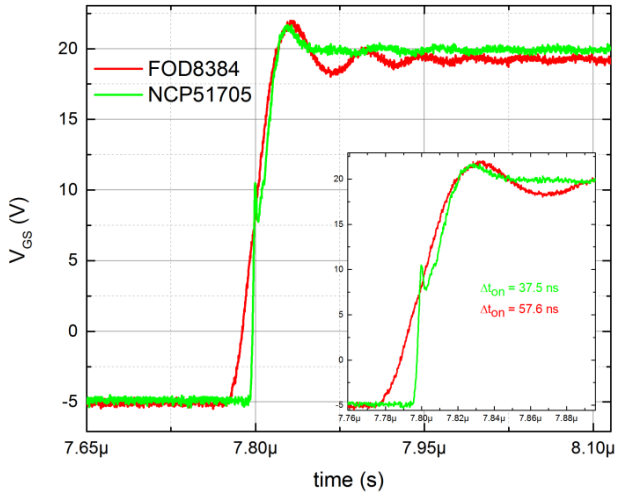

Figure 59. V_{GS} Rising Edge Comparison

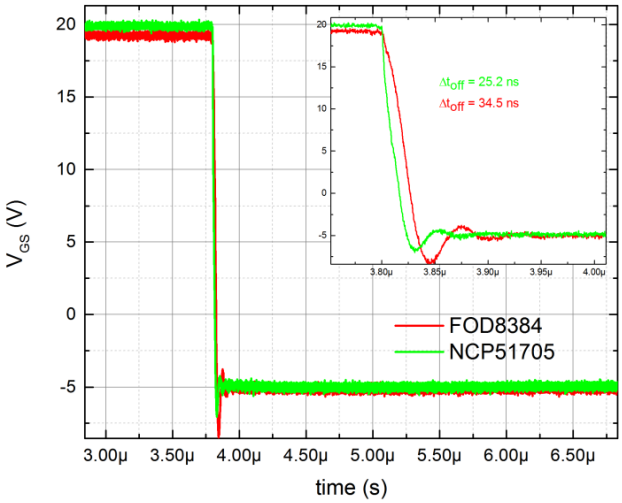

Figure 60. V_{GS} Falling Edge Comparison

A well designed gate driver IC includes low source and sink impedance so that the SiC MOSFET drain can be accurately controlled by the gate. Secondly, minimizing driver output impedance is essential for allowing the highest natural dV/dt of the SiC MOSFET. The natural dV/dt limit of a SiC MOSFET is inversely proportional to R_{LO} + R_{GATE} + R_{GI}. When R_{LO} is higher than necessary, the natural dV/dt limit of the SiC MOSFET is lowered. This makes the device more susceptible to dV/dt induced turn−on and limits the amount of dV_{DS}/dt control that can be achieved by the selection of R_{GATE}. The NCP51705 V_{DS} waveforms shown in Figure 61 reveal the high degree of dV_{DS}/dt control that is possible by simply varying R_{GATE}. For R_{GATE} = 1 Ω, dV_{DS}/dt = 72 V/ns. Increasing R_{GATE} from 1 Ω to 15 Ω reduces dV_{DS}/dt from 72 V/ns to 68 V/ns. This demonstrates that a much higher R_{GATE} can be used to obtain very fine incremental steps toward reducing dV_{DS}/dt, if desired.

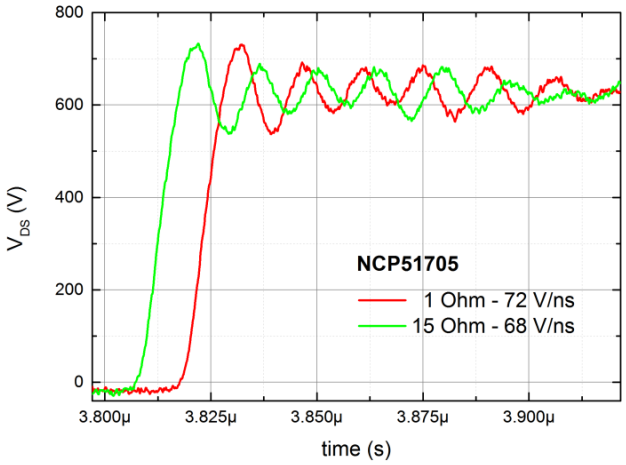

Figure 61. NCP51705 V_{DS} Rising Edge, Vary Gate Resistance

The same experiment was completed using the FOD8384 opto gate driver. Notice from the waveforms shown in Figure 62, a change in R_{GATE} from 1 Ω to 15 Ω, results in a dV_{DS}/dt rate change by more than 2:1. dV_{DS}/dt control is more influenced by smaller changes in R_{GATE} due to the higher output impedance of the FOD8384 driver. Also, notice the dV_{DS}/dt rise of the NCP51705 is more linear comparatively.

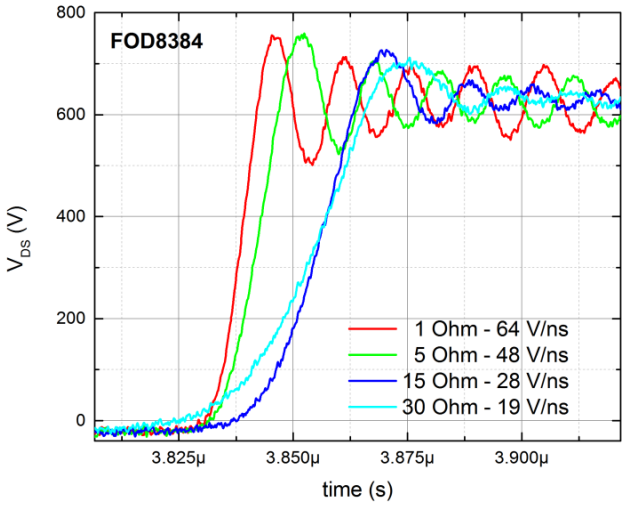

Figure 62. FOD8384 V_{DS} Rising Edge, Vary Gate Resistance

The waveforms shown in Figure 63 compare V_{DS} for each driver switching the same load from −5 V < V_{GS} < 20 V with R_{GATE} = 1 Ω. The dV_{DS}/dt rates are comparable at 72 V/ns verses 64 V/ns. The NCP51705 shows better damping and lower amplitude ringing.

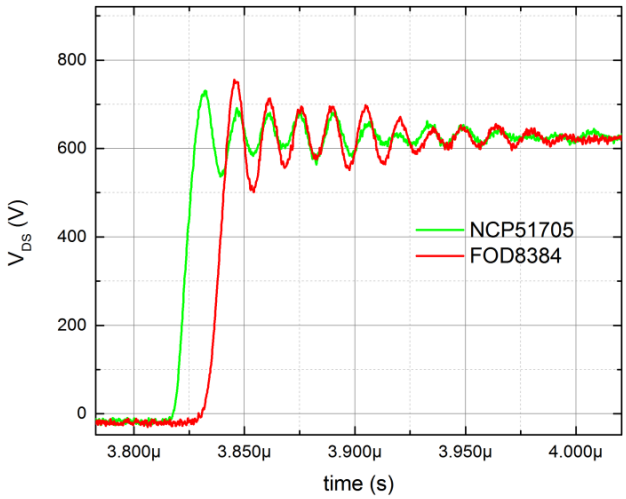

Figure 63. V_{DS} Rising Edge Compare, 1 Ω Gate Resistance

Another way the NCP51705 enables dV_{DS}/dt control is by varying the level of negative amplitude of V_{EE}. This can be done by configuring the VEESET pin according to Table 2 or by using an external negative DC power supply applied to V_{EE}. The waveforms in Figure 64 show the change in dV_{DS}/dt as V_{EE} is varied between −6 V < V_{EE} < 0 V. Notice the strong inflection and capacitive nature at low V_{DS}, for the case that 0 V < V_{GS} < 20 V. This is due to some residual gate charge from the SiC MOSFET not being fully turned off and highlights the importance of driving V_{GS} negative during turn−off.

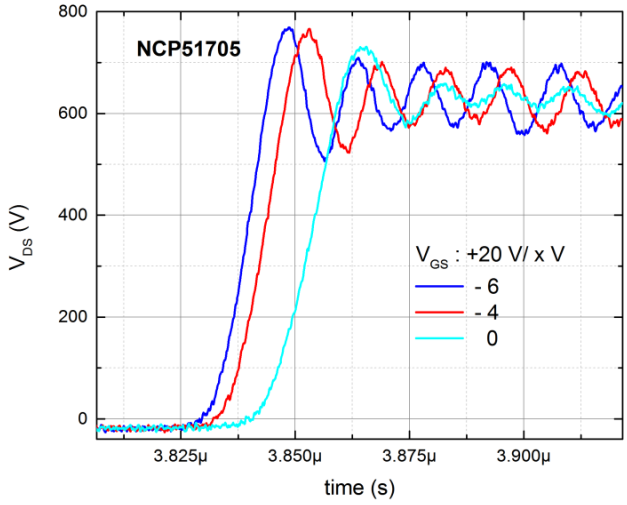

Figure 64. NCP51705 V_{DS} Rising Edge, Vary V_{EE}

The drain current measurements shown in Figure 65 were taken using a Pearson current probe. The NCP51705 current is falling at dI_D/dt = 3.2 A/ns yet exhibits less ringing compared to the FOD8384 drive circuit. The faster dI_D/dt of the NCP51705 correlates well to the V_{GS} falling edge waveforms shown in Figure 60.

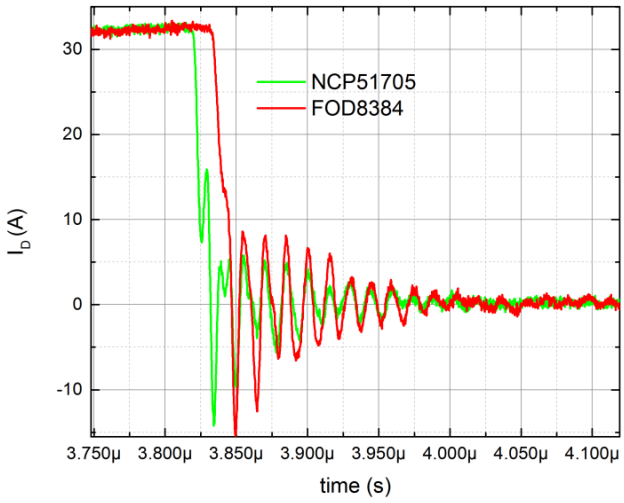

Figure 65. I_D Falling Edge Comparison

The double pulse test methodology is a test procedure traditionally used to characterize dynamic switching performance of discrete power semiconductor devices. Since the applied V_{DS} and initial I_D can be accurately controlled during turn−on and turn−off, this measuring technique has been shown to be a reliable method for characterizing gate driver IC performance in a clamped inductive switching application circuit.

References

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[2] Lutz
[3] Lutz et. al; 2017; 377−378

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